



H81H3-LM

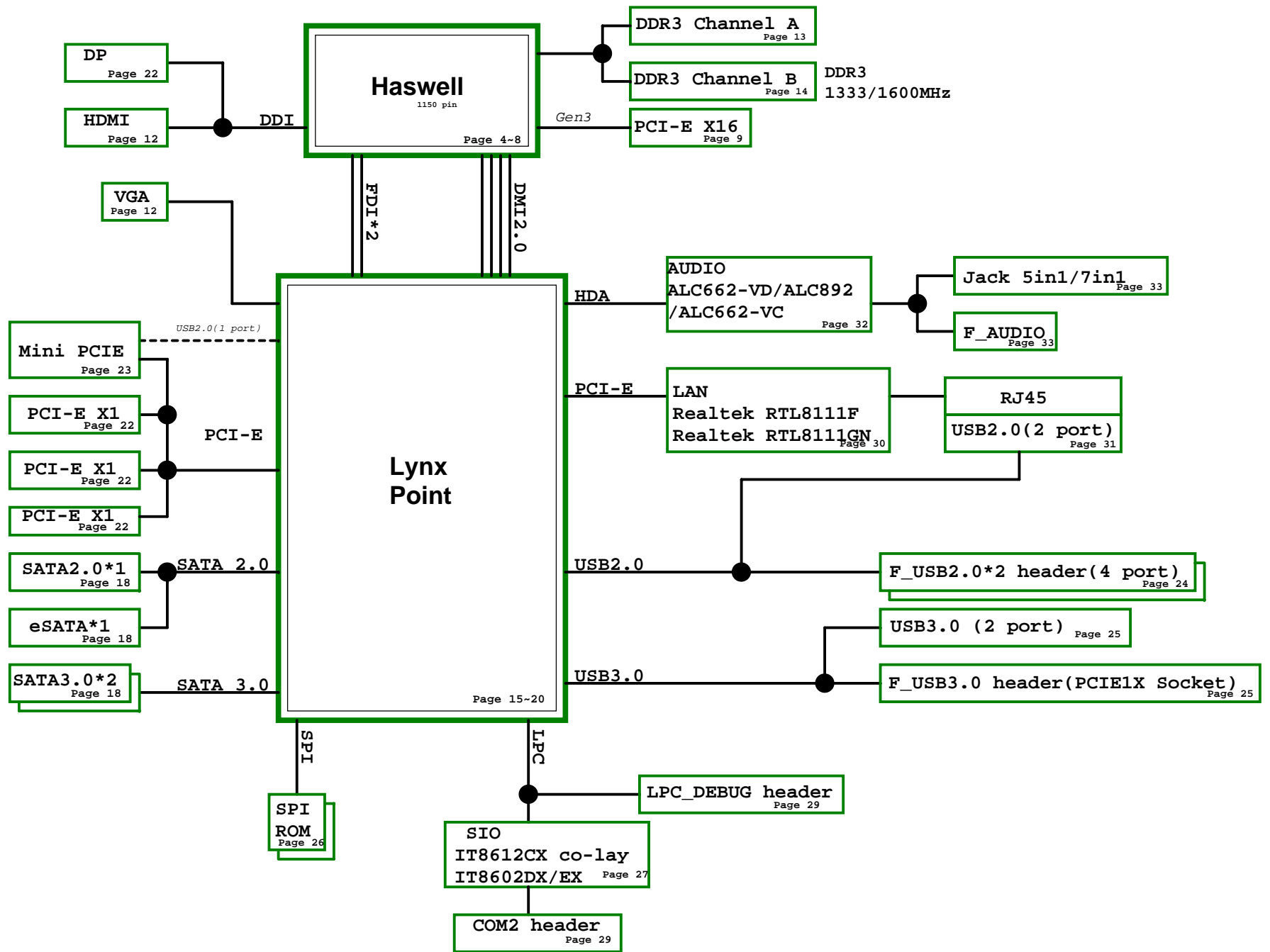
Shark Bay

Rev:1.0
IPG

ECS
CONFIDENTIAL

TABLE OF CONTENTS

Page	Index	Page	Index
1	Cover Page	27	SIO-IT8612CX/IT8602DX/EX
2	Block Diagram	28	FAN/F_Panel
3	GPIO Function & INT# Mapping	29	COM//Buzzer
4	CPU-PEG/DMI/FDI/DDI	30	LAN RTL8111GN Colay RTL8111F
5	CPU-MISC	31	LANUSB CONN
6	CPU-DDR3	32	Audio ALC662 Colay ALC892
7	CPU-POWER	33	AUDIO-CONN & Header
8	CPU-GND	34	XDP-CPU/PCH
9	PCIE*16	35	DC/DC VDIMM/DDR_VTT/5VDUAL
10	VGA/HDMI	36	VCC3&VCC
11	LEVEL_SHIFT ASM1442	37	DC/DC PCH_1.5V/PCH_1.05V/ATX_3VSB
12	DDR3-CHA	38	DC/DC Vcore_Controller
13	DDR3-CHB	39	DC/DC Vcore_Gate Driver
14	DDR3-Vref	40	PWR Delivery
15	PCH-DMI/PE/USB2.0	41	PWR Sequence/RST Diagram
16	PCH-FDI/DDI/USB3.0/CLK/VGA	42	CLK Distribution
17	PCH-SATA/SATA connector	43	REVISION HISTORY
18	PCH-MISC		
19	PCH-POWER		
20	PCH-GND		
21	PCIE1X*3		
22	Mini_PCIE/DP		
23	USB2.0 Header		
24	USB3.0 Conn & Header		
25	USB Charge		
26	SPI/SMbus/USB Discharge		



PCH-GPIO function

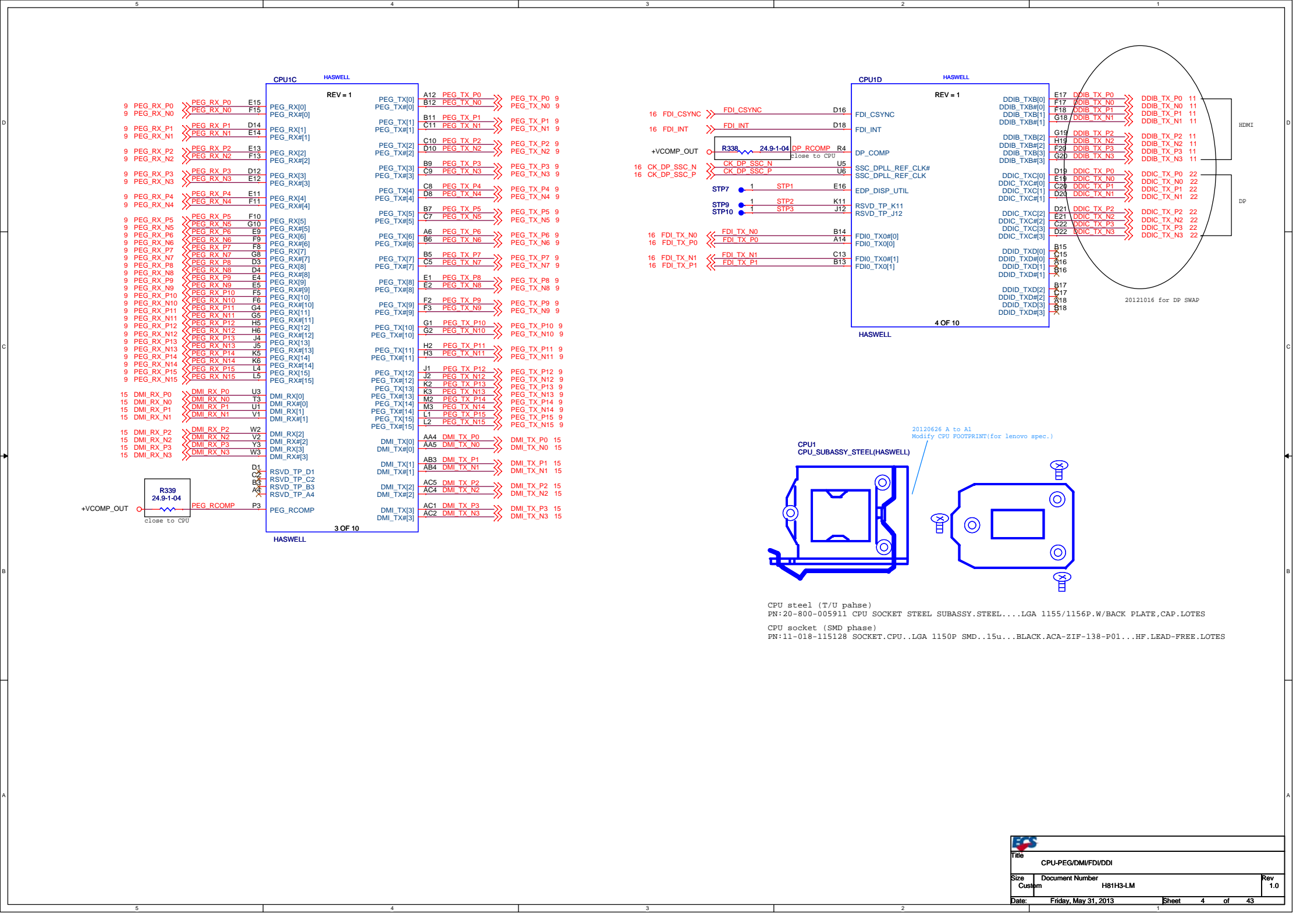
Pin Name	Power Well	Usage	Default Status	Boot Set
GPIO13	3VSB	PCH_GPIO13 (USB Charger CTL1)	GPI	GPO
GPIO14	3VSB	TS_F	OC7#	GPI
GPIO15	3VSB	PCIE16X_RST_L	GPO	GPI
GPIO22	VCC3	SW_CLR_CMOS	GPI	GPI
GPIO24	3VSB	ME disable	GPO	GPO
GPIO25	3VSB	PCH_GPIO25 (USB Charger CTL3)	PCIECLKRQ3#	GPO
GPIO26	3VSB	PCH_GPIO26 (USB Charger CTL4)	PCIECLKRQ4#	GPO
GPIO27	+ATX_3VSB	MS_GP0(Mode_Switch)	GPO	GPI
GPIO28	+ATX_3VSB	MS_GP1(Mode_Switch)	GPO	GPI
GPIO29	3VSB	PCH_GPIO29(BOM detect)	GPI	GPI
GPIO31	3VSB	PCH_GPIO31(+VDIMM select)	GPI	GPO
GPIO39	VCC3	CAS0(SEN_HEADER)	GPI	GPI
GPIO45	3VSB	LAN_DIS_L(MINI_PCIE)	PCIECLKRQ6#	GPO
GPIO48	VCC3	CAS1(SEN_HEADER)	GPI	GPI
GPIO49	VCC3	PCH_GPIO49 USB/PCIE(mSATA) DET	GPI	GPO
GPIO50	VCC3	PS2_DET	GPI	GPI
GPIO52	VCC3	PCH_GPIO52 (FP_AUD_DETECT)	GPI	GPO
GPIO54	VCC3	COM_DET	GPI	GPI
GPIO57	3VSB	MODE_CTRL(Mode_Switch)	GPI	GPI
GPIO60	3VSB	PCH_GPIO60(BOM detect)	SML0ALERT#	GPI
GPIO64	VCC3	PCH_GPIO64(BOM detect)	CLKOUTFLEX0	GPI
GPIO65	VCC3	PCH_GPIO65(BOM detect)	CLKOUTFLEX1	GPI
GPIO66	VCC3	PCH_GPIO66(BOM detect)	CLKOUTFLEX2	GPI
GPIO73	3VSB	PCH_GPIO73	PCIECLKRQ0#	GPI
GPIO74	3VSB	PCH_GPIO74(BOM detect)	SML1ALERT#	GPI

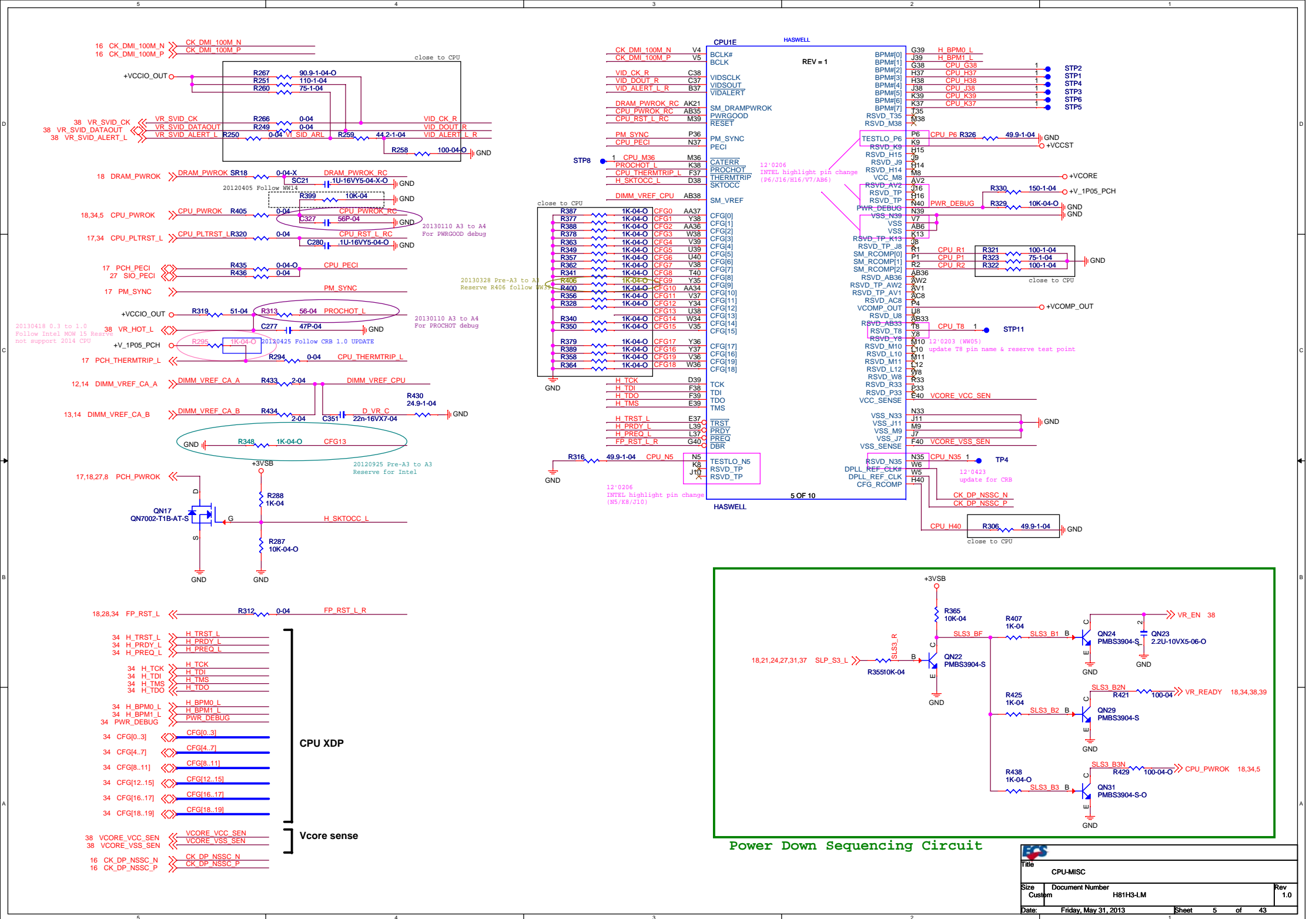
SIO-GPIO function

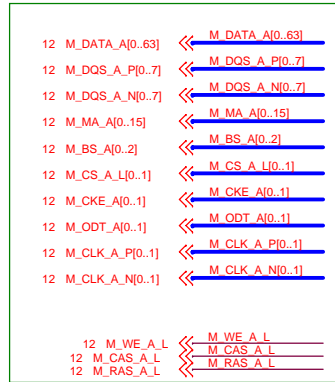
Pin Name	Power Well	Usage	Default SET
GP12	VCC3	PCIRST1_L	GPO
GP22	3VSB	SIO_LED0	GPIO
GP43	3VSB	SIO_LED1	GPIO
GP56	VCC3	TS_F	GPIO

Interrupt mapping

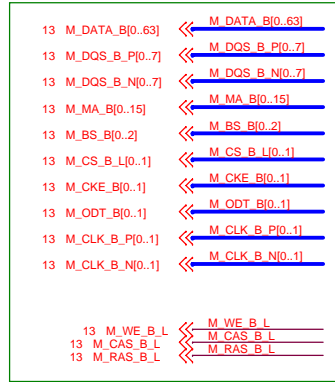
Function	INT# port	PCle*1 port	Device
LAN	INTC#	port 3	RTL8111GN
PCIE1X_1	INTB#	port 2	LPT integrate
PCIE1X_2	INTD#	port 4	LPT integrate
PCIE1X_3	INTA#	port 5	LPT integrate
mini-PCIE	INTB#	port 6	LPT integrate
SATA	INTB#	N/A	LPT integrate







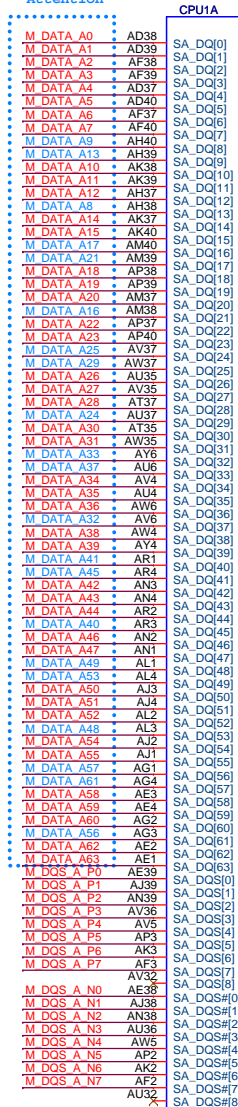
DDR3 CH.A



DDR3 CH.B

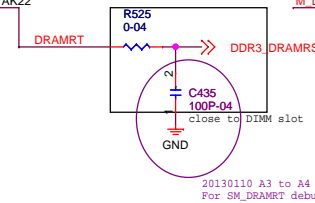
12,13,6 DDR3_DRAMRST_L << DDR3_DRAMRST_L

**Attention

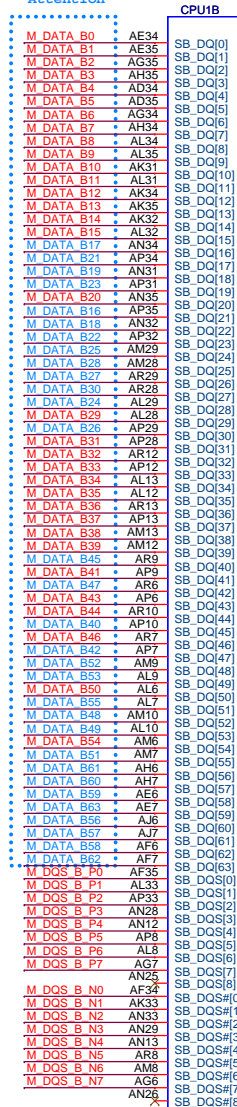


HASWELL

1 OF 10

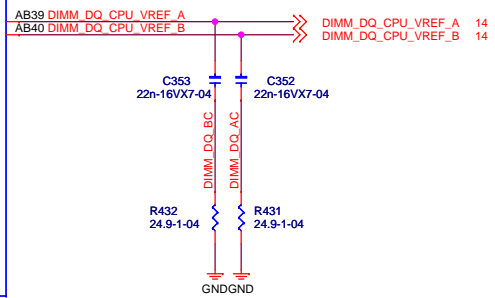


**Attention



HASWELL

2 OF 10



20130418 0.3 to 1.0
Follow Intel MW 15 Reserve
not support 2014 CPU

+VCCIO_OUT

+V_1P05_PCH

20120425 Follow CRB 1.0 UPDATE

R303
0-04-O

R315
0-04

0-04-X-O

+VCCIO_PCH

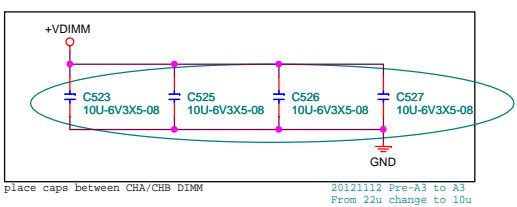
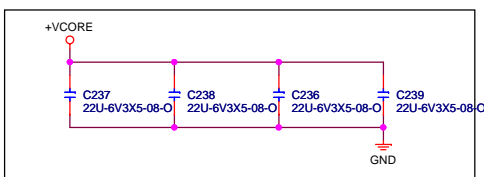
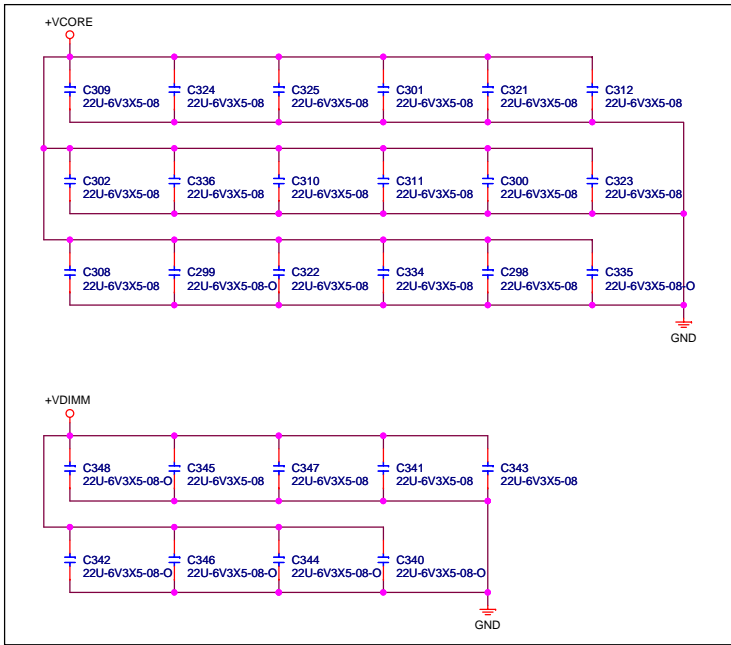
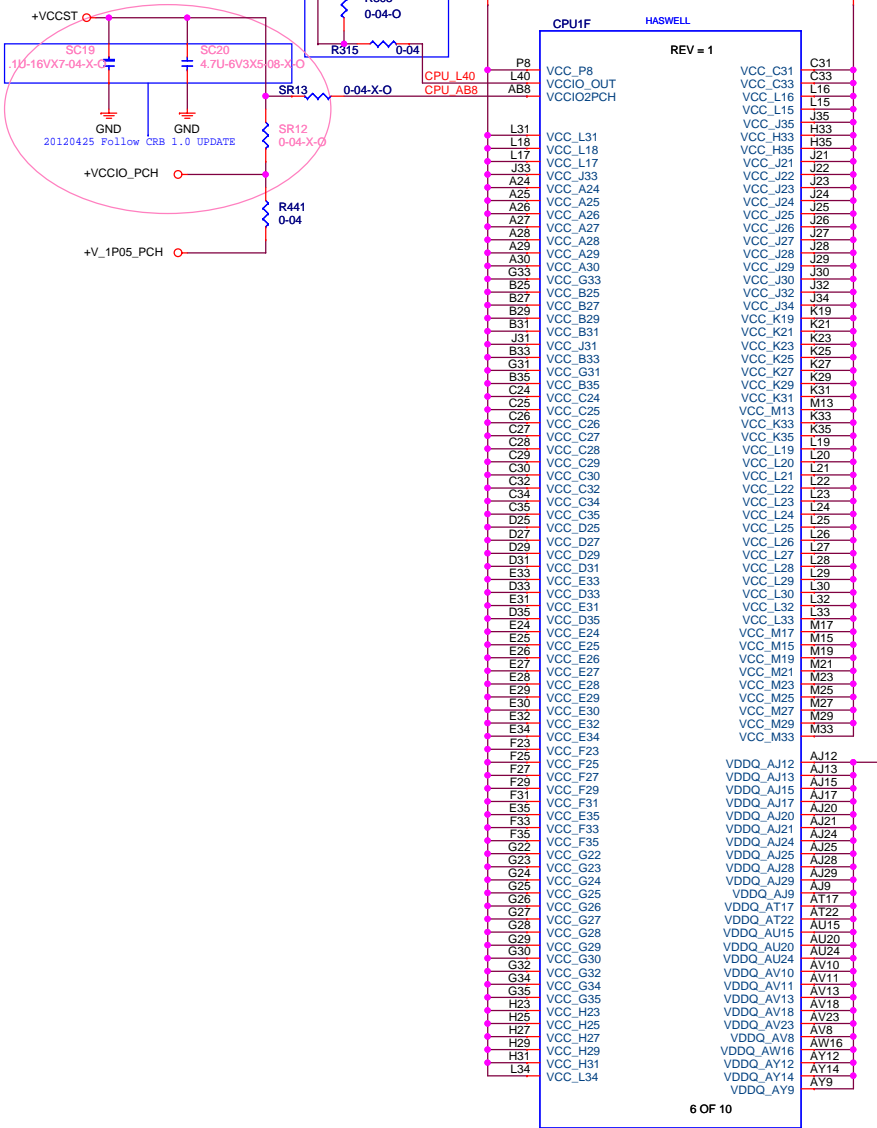
+V_1P05_PCH

20120425 Follow CRB 1.0 UPDATE

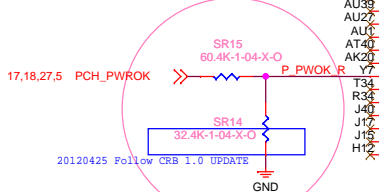
SR13
0-04-X-O

SR12
0-04-X-O

R441
0-04



20130418 0.3 to 1.0
Follow Intel MOW 15 Reserve
not support 2014 CPU



note.Y7 pin is VCCST PWRGD only for 2014 processors
and need divider to meet 1.05V level
refer to PDG_V1.0 section 38.4

CPU1H		HASWELL	
REV = 1			
RSVD_TP_K12	X12	RSVD_TP_K12	X12
RSVD_TP_J13	X13	RSVD_TP_J13	X13
RSVD_TP_P37	P37	RSVD_TP_P37	P37
RSVD_TP_N38	N38	RSVD_TP_N38	N38
IVR-ERROR	X39	IVR-ERROR	X39
RSVD_TP_C39	X39	RSVD_TP_C39	X39
VSS_U35	U35	VSS_U35	U35
VSS_P40	P40	VSS_P40	P40
VSS_R38	R38	VSS_R38	R38
VSS_T37	T37	VSS_T37	T37
VSS_V34	V34	VSS_V34	V34
VSS_R39	R39	VSS_R39	R39
VSS_T38	T38	VSS_T38	T38
VSS_U36	U36	VSS_U36	U36
VSS_P39	P39	VSS_P39	P39
VSS_T36	T36	VSS_T36	T36
VSS_R37	R37	VSS_R37	R37
VSS_J14	J14	VSS_J14	J14
RSVD_TP_N36	N36	RSVD_TP_N36	N36

CPU1G		HASWELL	
REV = 1			
VSS_AP11	AP11	VSS_AP11	AP11
VSS_AP14	AP14	VSS_AP14	AP14
VSS_AP15	AP15	VSS_AP15	AP15
VSS_AP24	AP24	VSS_AP24	AP24
VSS_AP27	AP27	VSS_AP27	AP27
VSS_AP30	AP30	VSS_AP30	AP30
VSS_AP36	AP36	VSS_AP36	AP36
VSS_AP4	AP4	VSS_AP4	AP4
VSS_AP5	AP5	VSS_AP5	AP5
VSS_AP11	AP11	VSS_AP11	AP11
VSS_AR14	AR14	VSS_AR14	AR14
VSS_AR16	AR16	VSS_AR16	AR16
VSS_AR17	AR17	VSS_AR17	AR17
VSS_AR18	AR18	VSS_AR18	AR18
VSS_AR19	AR19	VSS_AR19	AR19
VSS_AR20	AR20	VSS_AR20	AR20
VSS_AR21	AR21	VSS_AR21	AR21
VSS_AR22	AR22	VSS_AR22	AR22
VSS_AR23	AR23	VSS_AR23	AR23
VSS_AR24	AR24	VSS_AR24	AR24
VSS_AR27	AR27	VSS_AR27	AR27
VSS_AR30	AR30	VSS_AR30	AR30
VSS_AR31	AR31	VSS_AR31	AR31
VSS_AR32	AR32	VSS_AR32	AR32
VSS_AR33	AR33	VSS_AR33	AR33
VSS_AR34	AR34	VSS_AR34	AR34
VSS_AR35	AR35	VSS_AR35	AR35
VSS_AR36	AR36	VSS_AR36	AR36
VSS_AR37	AR37	VSS_AR37	AR37
VSS_AR38	AR38	VSS_AR38	AR38
VSS_AR39	AR39	VSS_AR39	AR39
VSS_AR40	AR40	VSS_AR40	AR40
VSS_AR5	AR5	VSS_AR5	AR5
VSS_AT1	AT1	VSS_AT1	AT1
VSS_AT10	AT10	VSS_AT10	AT10
VSS_AT11	AT11	VSS_AT11	AT11
VSS_AT12	AT12	VSS_AT12	AT12
VSS_AT13	AT13	VSS_AT13	AT13
VSS_AT14	AT14	VSS_AT14	AT14
VSS_AT15	AT15	VSS_AT15	AT15
VSS_AT16	AT16	VSS_AT16	AT16
VSS_AT2	AT2	VSS_AT2	AT2
VSS_AT24	AT24	VSS_AT24	AT24
VSS_AT25	AT25	VSS_AT25	AT25
VSS_AT26	AT26	VSS_AT26	AT26
VSS_AT27	AT27	VSS_AT27	AT27
VSS_AT28	AT28	VSS_AT28	AT28
VSS_AT29	AT29	VSS_AT29	AT29
VSS_AT3	AT3	VSS_AT3	AT3
VSS_AT30	AT30	VSS_AT30	AT30
VSS_AT32	AT32	VSS_AT32	AT32
VSS_AT34	AT34	VSS_AT34	AT34
VSS_AT36	AT36	VSS_AT36	AT36
VSS_AT38	AT38	VSS_AT38	AT38
VSS_AT39	AT39	VSS_AT39	AT39
VSS_AT4	AT4	VSS_AT4	AT4
VSS_AT5	AT5	VSS_AT5	AT5
VSS_AT6	AT6	VSS_AT6	AT6
VSS_AT7	AT7	VSS_AT7	AT7
VSS_AT8	AT8	VSS_AT8	AT8
VSS_AT9	AT9	VSS_AT9	AT9
VSS_AU2	AU2	VSS_AU2	AU2
VSS_AU25	AU25	VSS_AU25	AU25
VSS_AU3	AU3	VSS_AU3	AU3
VSS_AU30	AU30	VSS_AU30	AU30
VSS_AU34	AU34	VSS_AU34	AU34
VSS_AU38	AU38	VSS_AU38	AU38
VSS_AU5	AU5	VSS_AU5	AU5
VSS_AU7	AU7	VSS_AU7	AU7
VSS_AV21	AV21	VSS_AV21	AV21
VSS_AV28	AV28	VSS_AV28	AV28
VSS_AV3	AV3	VSS_AV3	AV3
VSS_AV30	AV30	VSS_AV30	AV30
VSS_AV34	AV34	VSS_AV34	AV34
VSS_AV38	AV38	VSS_AV38	AV38
VSS_AV7	AV7	VSS_AV7	AV7
VSS_AV26	AV26	VSS_AV26	AV26
VSS_AW3	AW3	VSS_AW3	AW3
VSS_AW30	AW30	VSS_AW30	AW30

CPU1I		HASWELL	
REV = 1			
VSS_AW32	AW32	VSS_AW32	AW32
VSS_AW34	AW34	VSS_AW34	AW34
VSS_AW36	AW36	VSS_AW36	AW36
VSS_AW7	AW7	VSS_AW7	AW7
VSS_AW17	AW17	VSS_AW17	AW17
VSS_AY23	AY23	VSS_AY23	AY23
VSS_AY26	AY26	VSS_AY26	AY26
VSS_AY27	AY27	VSS_AY27	AY27
VSS_AY30	AY30	VSS_AY30	AY30
VSS_AY5	AY5	VSS_AY5	AY5
VSS_AY7	AY7	VSS_AY7	AY7
VSS_B24	B24	VSS_B24	B24
VSS_B26	B26	VSS_B26	B26
VSS_B28	B28	VSS_B28	B28
VSS_B30	B30	VSS_B30	B30
VSS_B34	B34	VSS_B34	B34
VSS_B36	B36	VSS_B36	B36
VSS_B4	B4	VSS_B4	B4
VSS_B8	B8	VSS_B8	B8
VSS_C4	C4	VSS_C4	C4
VSS_C6	C6	VSS_C6	C6
VSS_C12	C12	VSS_C12	C12
VSS_C14	C14	VSS_C14	C14
VSS_C16	C16	VSS_C16	C16
VSS_C18	C18	VSS_C18	C18
VSS_C19	C19	VSS_C19	C19
VSS_C21	C21	VSS_C21	C21
VSS_C23	C23	VSS_C23	C23
VSS_C36	C36	VSS_C36	C36
VSS_B10	B10	VSS_B10	B10
VSS_B23	B23	VSS_B23	B23
VSS_C3	C3	VSS_C3	C3
VSS_C9	C9	VSS_C9	C9
VSS_D8	D8	VSS_D8	D8
VSS_D11	D11	VSS_D11	D11
VSS_D13	D13	VSS_D13	D13
VSS_D15	D15	VSS_D15	D15
VSS_D17	D17	VSS_D17	D17
VSS_D2	D2	VSS_D2	D2
VSS_D23	D23	VSS_D23	D23
VSS_D36	D36	VSS_D36	D36
VSS_D24	D24	VSS_D24	D24
VSS_D28	D28	VSS_D28	D28
VSS_D30	D30	VSS_D30	D30
VSS_D34	D34	VSS_D34	D34
VSS_D36	D36	VSS_D36	D36
VSS_D37	D37	VSS_D37	D37
VSS_D5	D5	VSS_D5	D5
VSS_D6	D6	VSS_D6	D6
VSS_D7	D7	VSS_D7	D7
VSS_E7	E7	VSS_E7	E7
VSS_E8	E8	VSS_E8	E8
VSS_E10	E10	VSS_E10	E10
VSS_E18	E18	VSS_E18	E18
VSS_E3	E3	VSS_E3	E3
VSS_E20	E20	VSS_E20	E20
VSS_E22	E22	VSS_E22	E22
VSS_E23	E23	VSS_E23	E23
VSS_E36	E36	VSS_E36	E36
VSS_E38	E38	VSS_E38	E38
VSS_E38	E38	VSS_E38	E38
VSS_B32	B32	VSS_B32	B32
VSS_E6	E6	VSS_E6	E6
VSS_F1	F1	VSS_F1	F1
VSS_F32	F32	VSS_F32	F32
VSS_F12	F12	VSS_F12	F12
VSS_F14	F14	VSS_F14	F14
VSS_F16	F16	VSS_F16	F16
VSS_F18	F18	VSS_F18	F18
VSS_F21	F21	VSS_F21	F21
VSS_F22	F22	VSS_F22	F22
VSS_F24	F24	VSS_F24	F24
VSS_F26	F26	VSS_F26	F26
VSS_F28	F28	VSS_F28	F28
VSS_F30	F30	VSS_F30	F30
VSS_F34	F34	VSS_F34	F34
VSS_F36	F36	VSS_F36	F36
VSS_F4	F4	VSS_F4	F4
VSS_D32	D32	VSS_D32	D32
VSS_F7	F7	VSS_F7	F7
VSS_G9	G9	VSS_G9	G9
VSS_G11	G11	VSS_G11	G11

AW32	A5
AW34	A7
AW36	A11
AW7	A13
AY17	A15
AY23	A17
AY26	A23
AY27	AA3
AY30	AA6
AY5	AA7
AY7	AA8
B24	AA33
B26	AA35
B28	AA38
B30	AB5
B34	AB7
B36	AB24
B4	AB37
B8	AC3
C4	AC6
C6	AC7
C12	AC33
C14	AC34
C16	AC35
C18	AC36
C19	AC37
C21	AC38
C23	AC39
C36	AC40
B10	AD1
B23	AD2
C3	AD3
D9	AD4
D11	AD5
D13	AD6
D15	AD7
D17	AD8
D2	AD33
D23	AE36
D24	AE5
D26	AE8
D28	AE33
D34	AE37
D36	AE40
D37	AF1
D5	AF4
D6	AF5
D7	AF8
E7	AF33
E8	AG7
E10	AG5
E18	AG8
E3	AG33
E20	AG36
E21	AG37
E23	AG38
E36	AG39
E38	AG40
B32	AH1
F1	AH2
F11	AH3
F32	AH4
F12	AH5
F14	AH8
F16	AH33
F19	AH36
F30	AJ11
F22	AJ14
F24	AJ16
F26	AJ18
F28	AJ19
F30	AJ22
F34	AJ23
F36	AJ26
F4	AJ27
D32	AJ30
F7	AJ31
G9	AJ32
G11	AJ33

PCIE SPEC

VCC3: 3A

12V: 5.5A

3VSB: 0.375A

20130411 A4 to A5

Change Name for Lenovo spec

20130322 A4 to A5

Change to GND

18,21,22,26 SMBCLK_STBY
18,21,22,26 SMBDATA_STBY

18,21,22,30 PCIE_WAKE_L

4 PEG_TX_P0
4 PEG_TX_N0

PEG_TX_P0 C193
PEG_TX_N0 C190

4 PEG_TX_P1
4 PEG_TX_N1

PEG_TX_P1 C203
PEG_TX_N1 C207

4 PEG_TX_P2
4 PEG_TX_N2

PEG_TX_P2 C210
PEG_TX_N2 C206

4 PEG_TX_P3
4 PEG_TX_N3

PEG_TX_P3 C213
PEG_TX_N3 C212

4 PEG_TX_P4
4 PEG_TX_N4

PEG_TX_P4 C220
PEG_TX_N4 C217

4 PEG_TX_P5
4 PEG_TX_N5

PEG_TX_P5 C235
PEG_TX_N5 C230

4 PEG_TX_P6
4 PEG_TX_N6

PEG_TX_P6 C247
PEG_TX_N6 C243

4 PEG_TX_P7
4 PEG_TX_N7

PEG_TX_P7 C259
PEG_TX_N7 C255

4 PEG_TX_P8
4 PEG_TX_N8

PEG_TX_P8 C274
PEG_TX_N8 C272

4 PEG_TX_P9
4 PEG_TX_N9

PEG_TX_P9 C282
PEG_TX_N9 C279

4 PEG_TX_P10
4 PEG_TX_N10

PEG_TX_P10 C294
PEG_TX_N10 C290

4 PEG_TX_P11
4 PEG_TX_N11

PEG_TX_P11 C318
PEG_TX_N11 C306

4 PEG_TX_P12
4 PEG_TX_N12

PEG_TX_P12 C337
PEG_TX_N12 C333

4 PEG_TX_P13
4 PEG_TX_N13

PEG_TX_P13 C354
PEG_TX_N13 C349

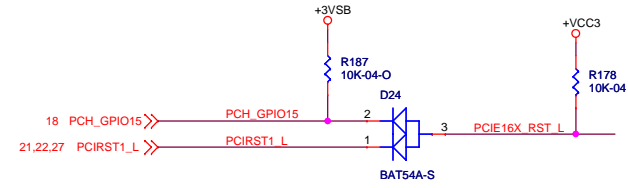
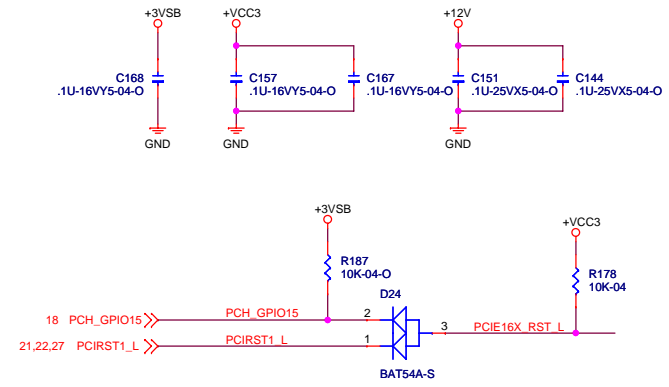
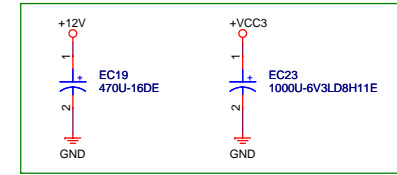
4 PEG_TX_P14
4 PEG_TX_N14

PEG_TX_P14 C360
PEG_TX_N14 C359

4 PEG_TX_P15
4 PEG_TX_N15

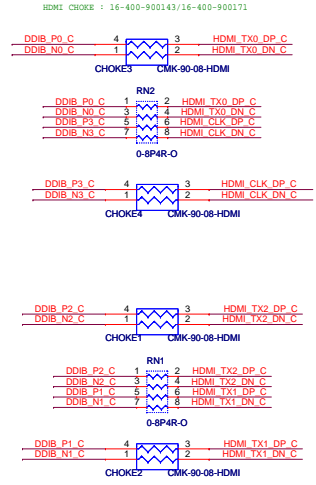
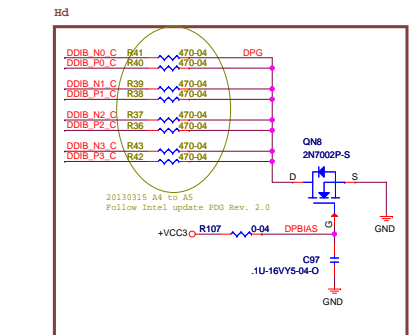
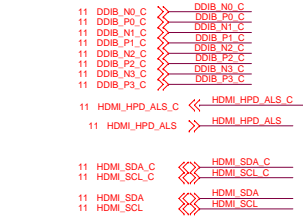
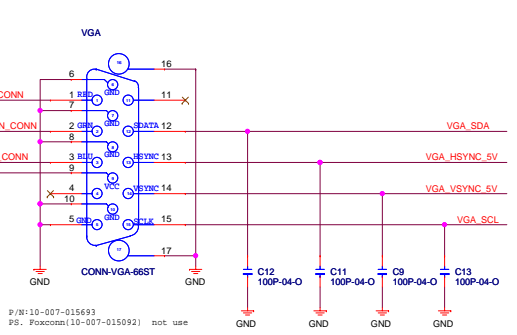
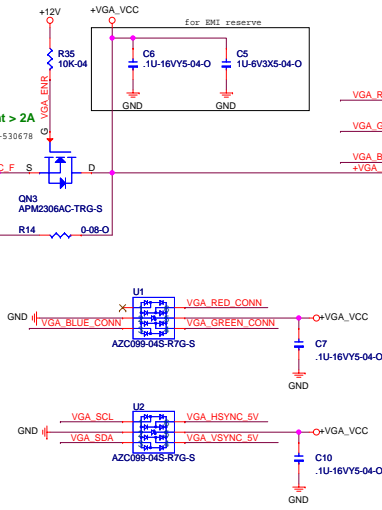
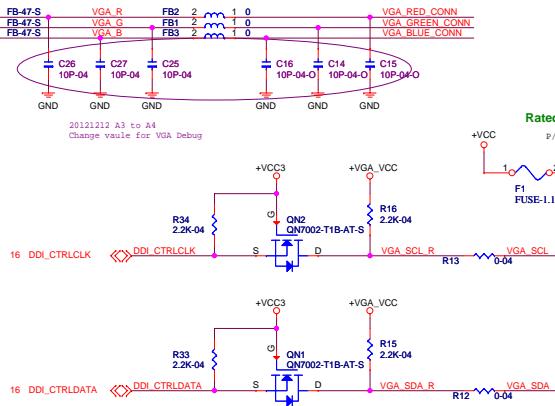
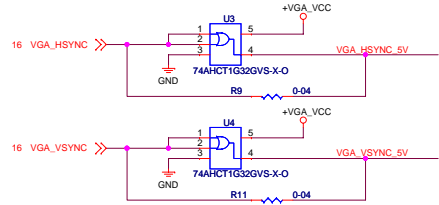
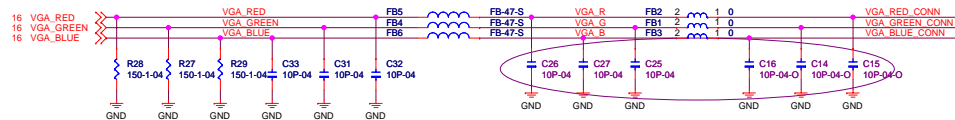
PEG_TX_P15 C367
PEG_TX_N15 C372

PCIE16-BK-LL15

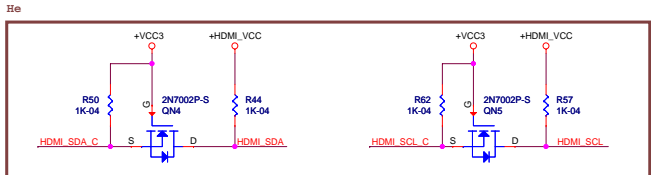
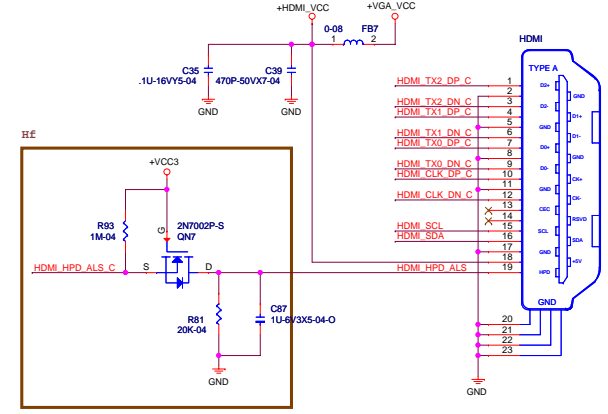
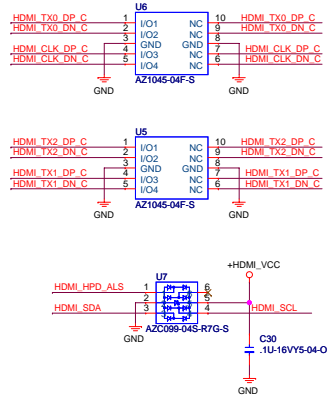


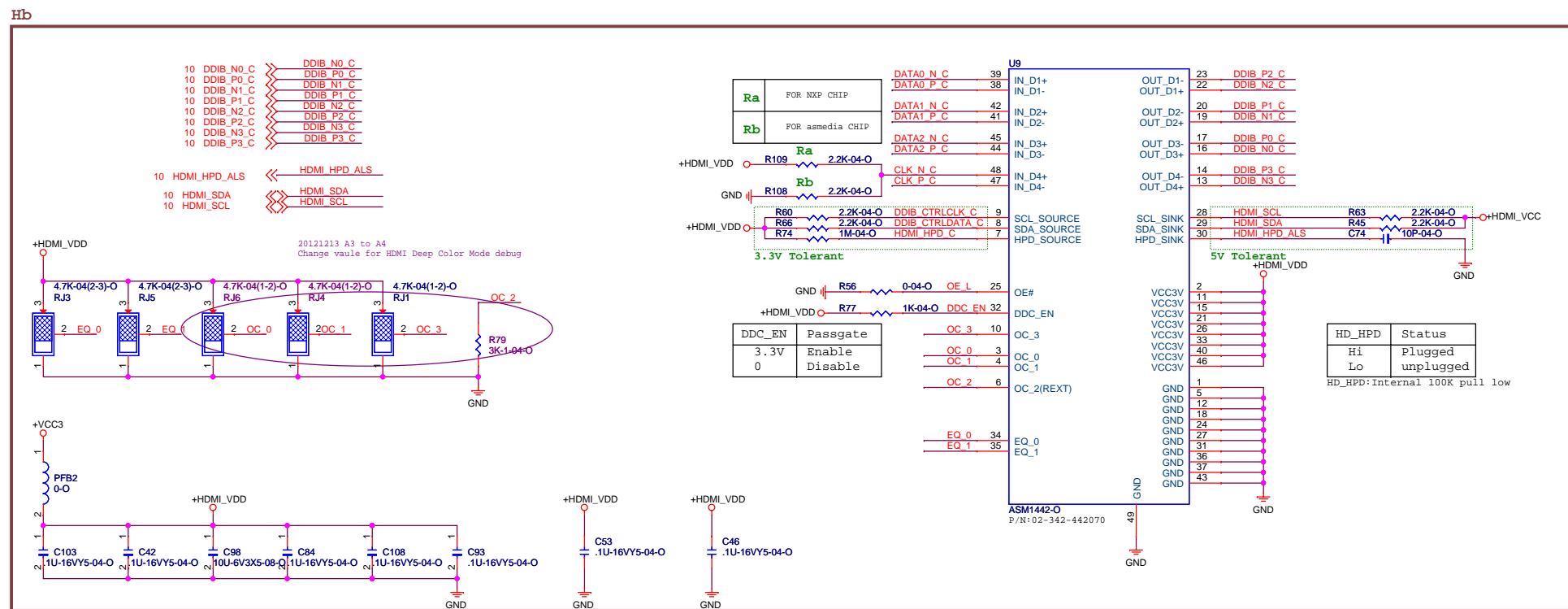
VGA

HDMI

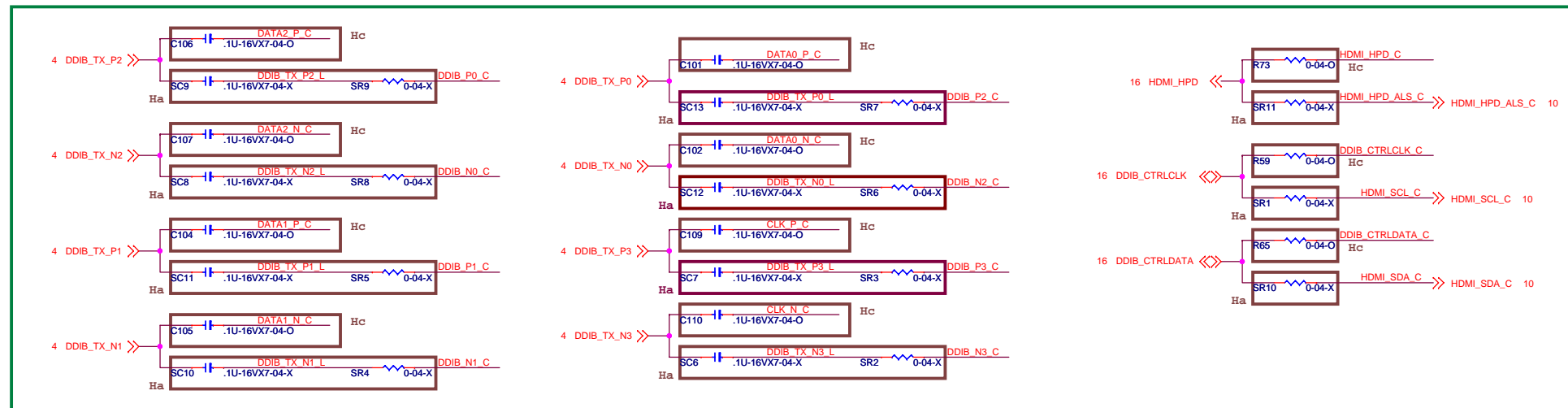


MODE	Ha	Hb	Hc	Hd	He	He
Level Shift	X	V	V	X	X	X
Non Level shift	V	X	X	V	V	V

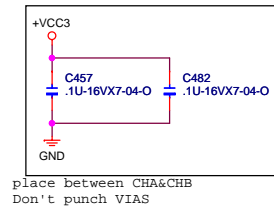
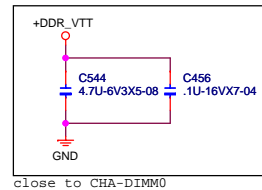
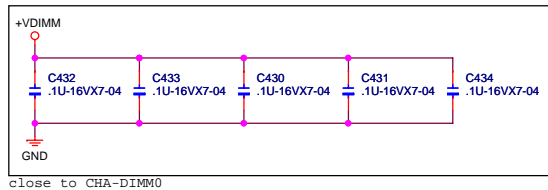
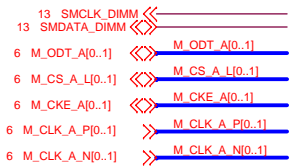


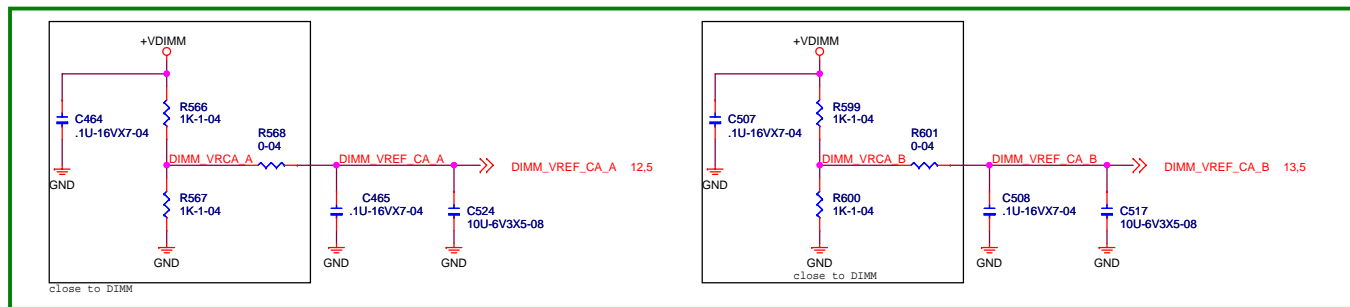


HDMI Signal Option Close (Level shift)ASM1442

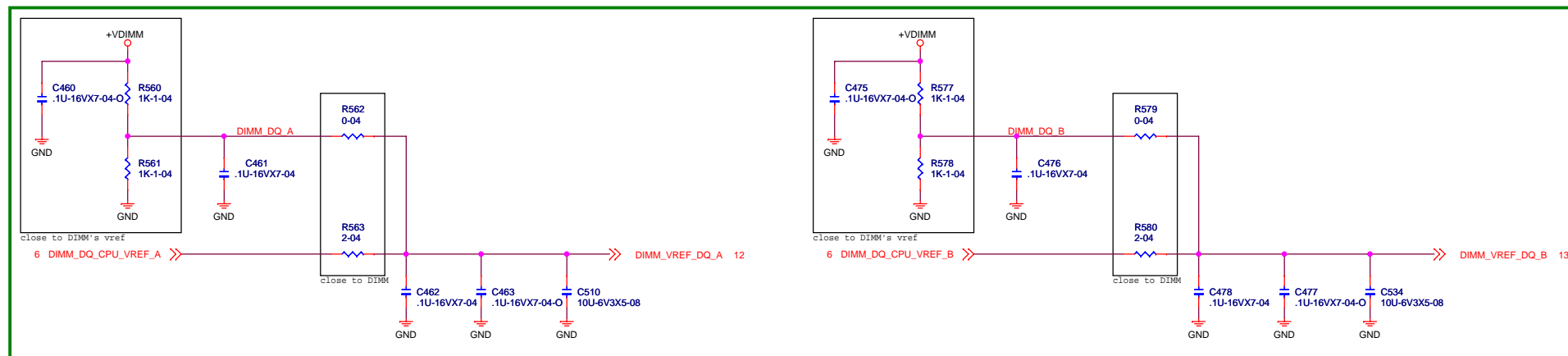


CHANNEL A DIMMs



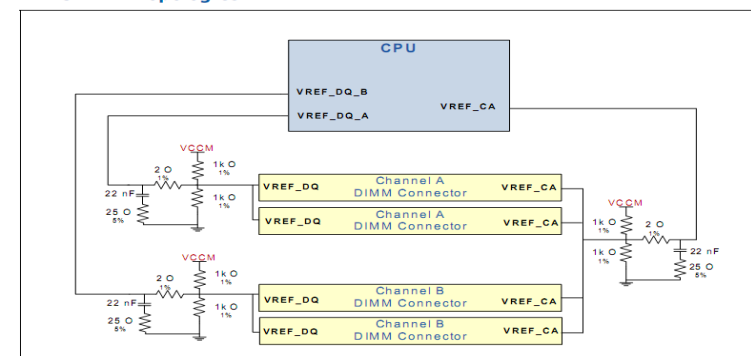


DIMM_VREF_CA Circuit



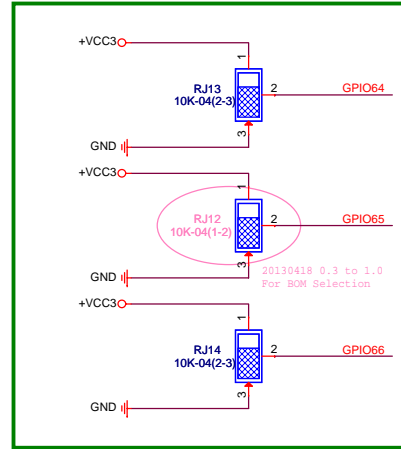
DIMM_VREF_DQ Circuit

Figure 4-8. DDR3 VREF Topologies



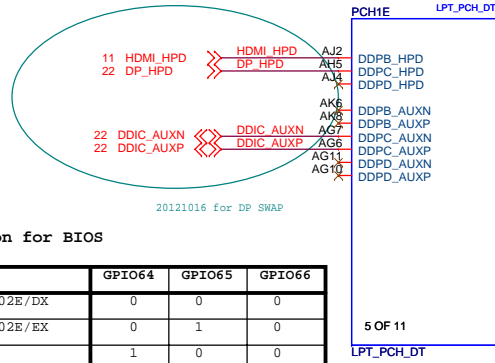
486711_486711_Shark_Bay_PDG_DT_rev0.9.pdf PAGE 67

Reserve for BIOS

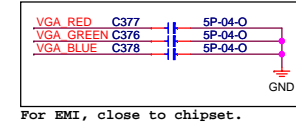


Selection for BIOS

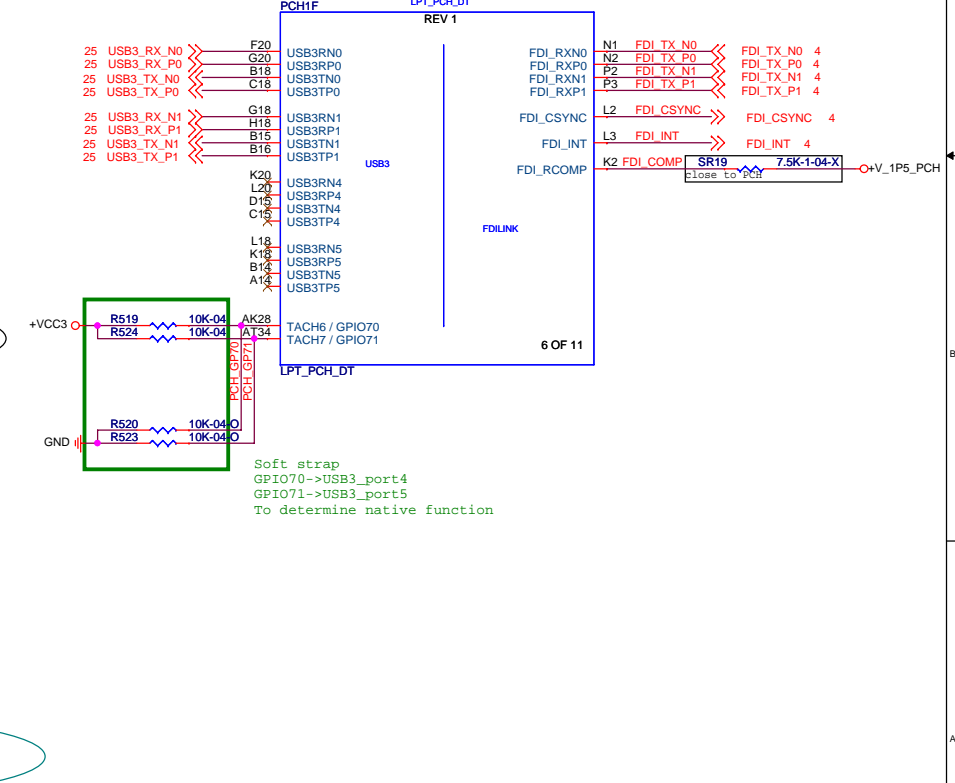
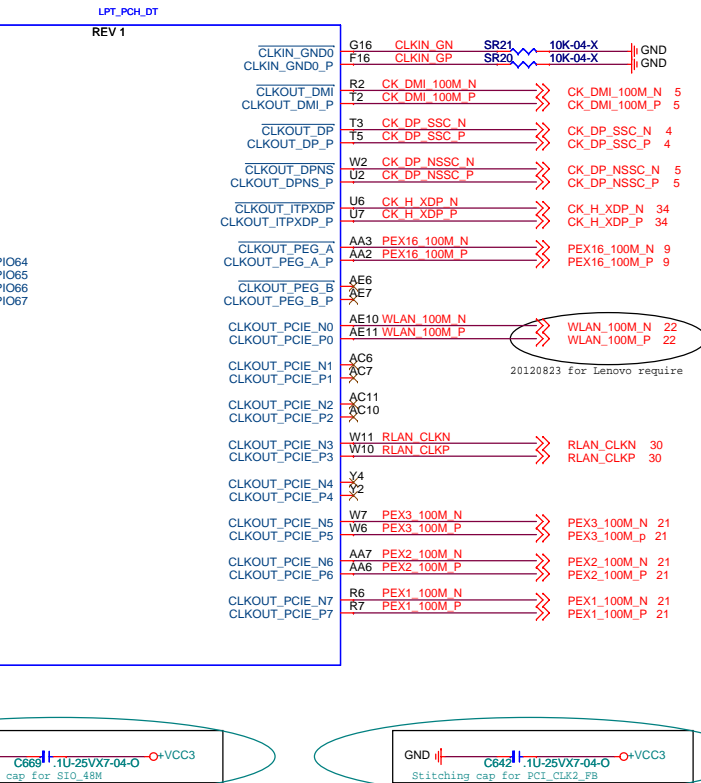
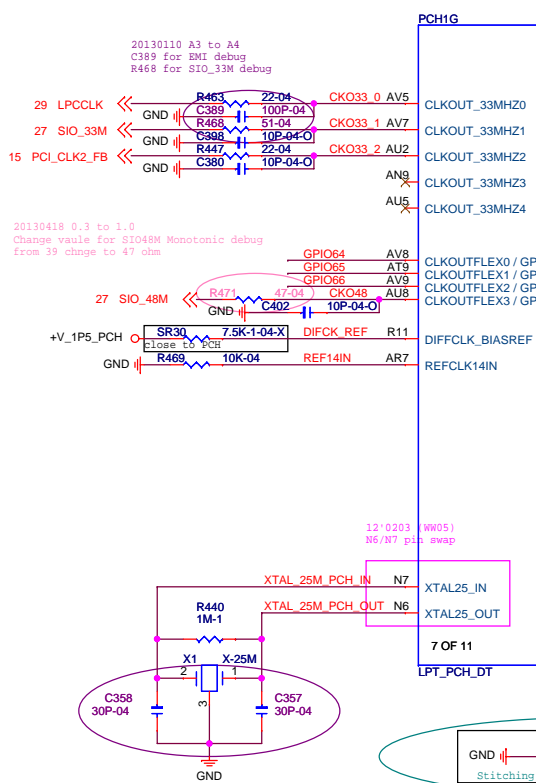
BOM	GPIO64	GPIO65	GPIO66
ALC662+8602E/DX	0	0	0
ALC662+8602E/EX	0	1	0
	1	0	0
	1	1	0

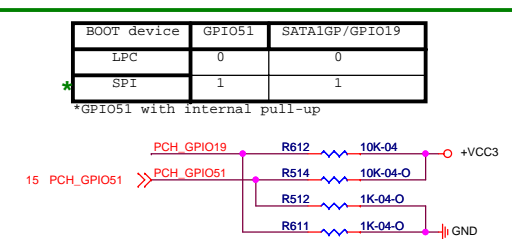
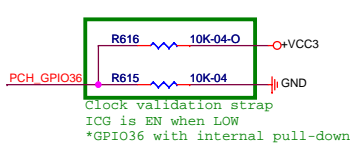
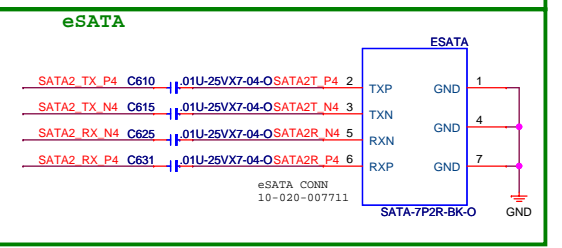
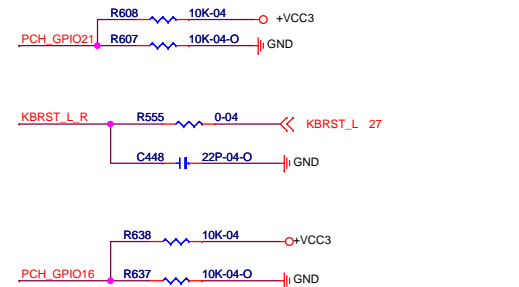



Layout note:
DDC_DATA要長於DDC_CLK約1inch.
越接近越好但不要超過。

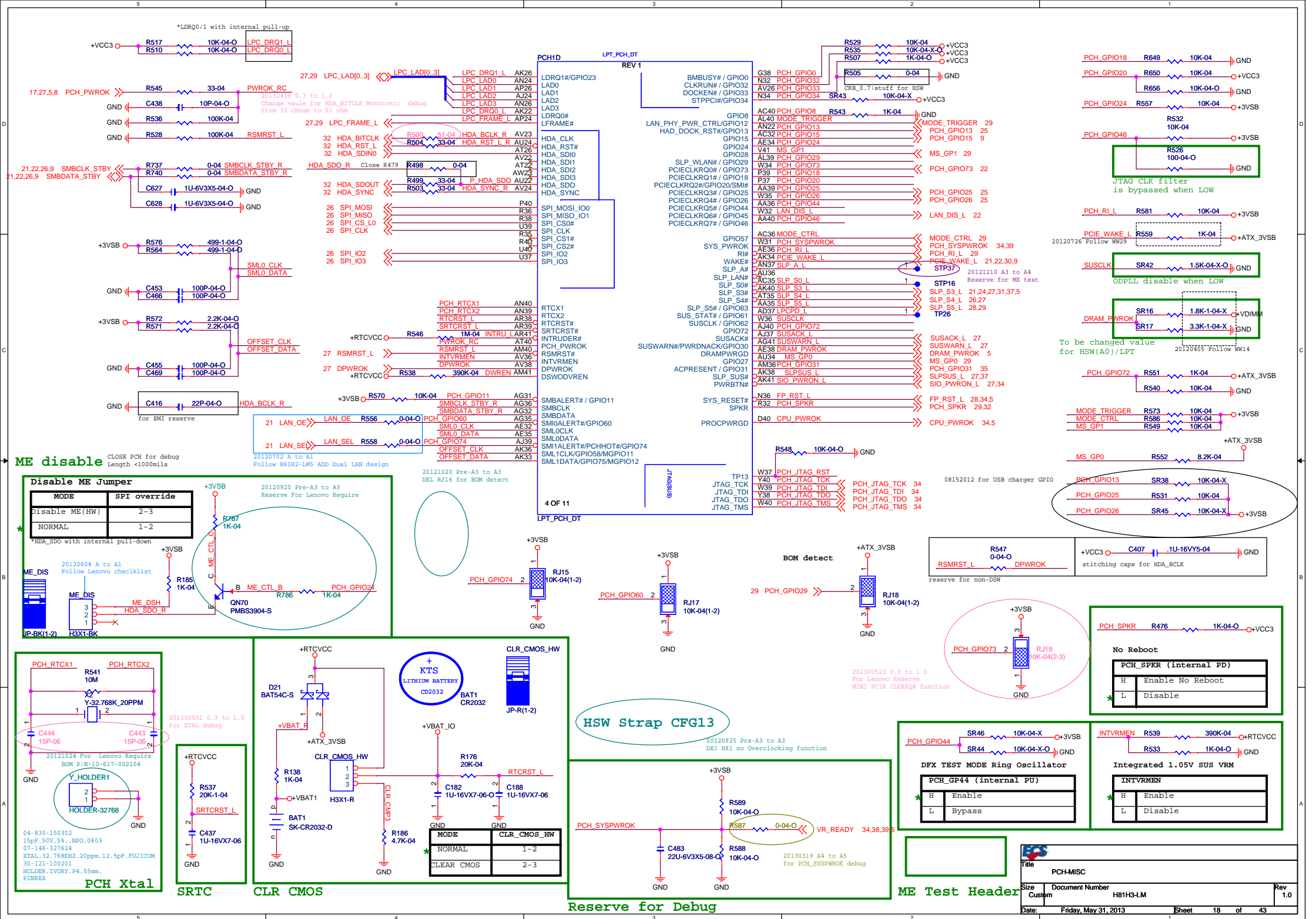


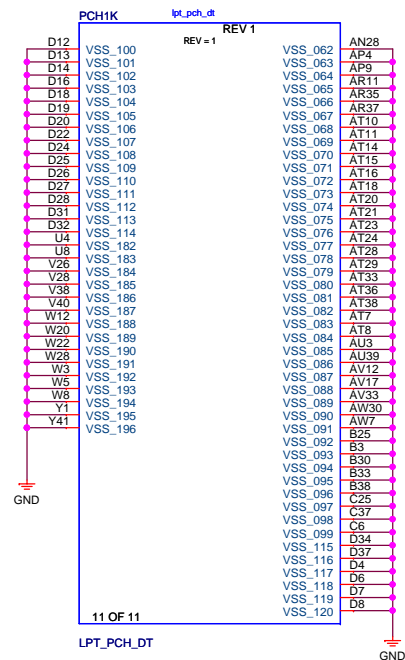
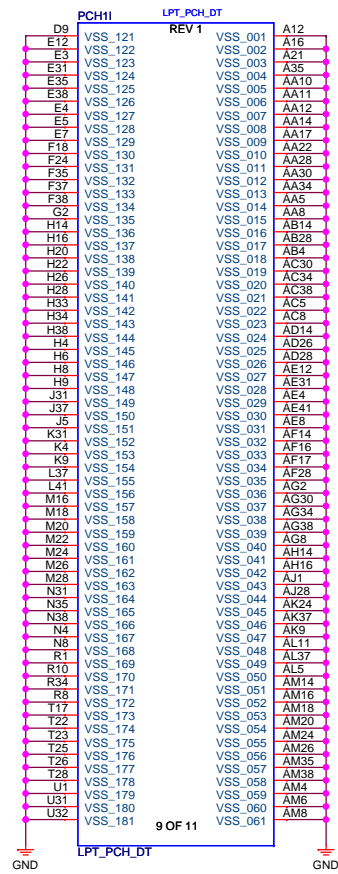
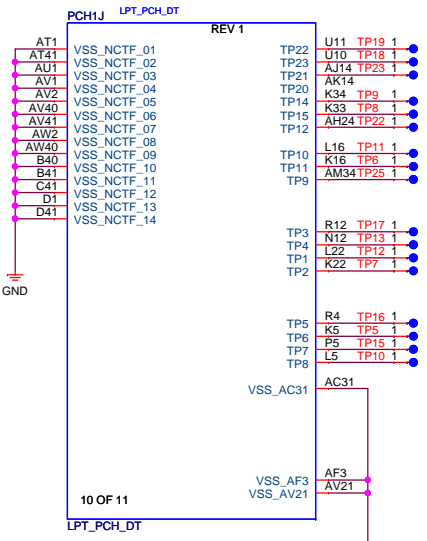
For EMI, close to chipset.





			
Title			
PCH-SATA/SATA connector			
Size	Document Number		Rev
Custom	H81H3-LM		1.0
Date:	Friday, May 31, 2013	Sheet	17 of 43





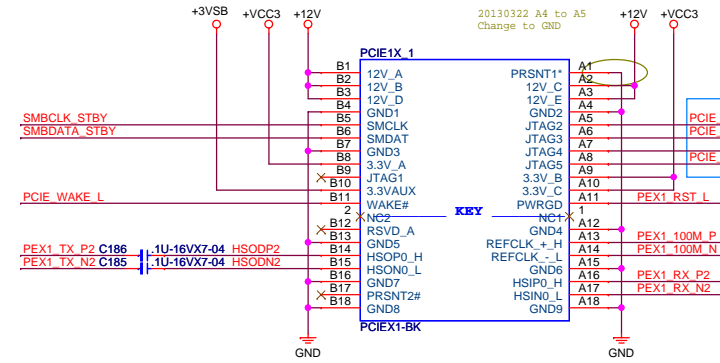
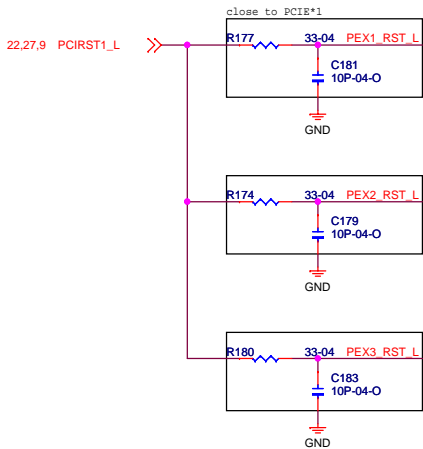
18,22,26,9 SMBCLK_STBY >> SMBCLK_STBY
18,22,26,9 SMBDATA_STBY >> SMBDATA_STBY
18,22,30,9 PCIE_WAKE_L >> PCIE_WAKE_L

16 PEX1_100M_P >> PEX1_100M_P
16 PEX1_100M_N >> PEX1_100M_N
16 PEX2_100M_P >> PEX2_100M_P
16 PEX2_100M_N >> PEX2_100M_N
16 PEX3_100M_P >> PEX3_100M_P
16 PEX3_100M_N >> PEX3_100M_N

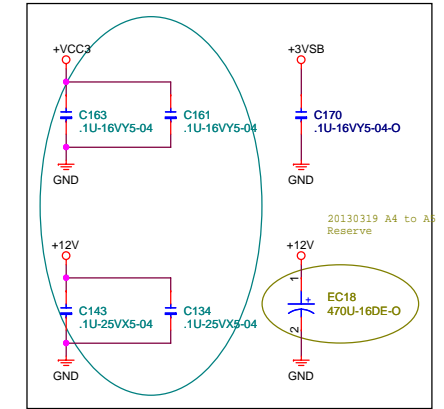
15 PEX1_TX_P2 >> PEX1_TX_P2
15 PEX1_TX_N2 >> PEX1_TX_N2
15 PEX1_RX_P2 >> PEX1_RX_P2
15 PEX1_RX_N2 >> PEX1_RX_N2

15 PEX1_TX_P4 >> PEX1_TX_P4
15 PEX1_TX_N4 >> PEX1_TX_N4
15 PEX1_RX_P4 >> PEX1_RX_P4
15 PEX1_RX_N4 >> PEX1_RX_N4

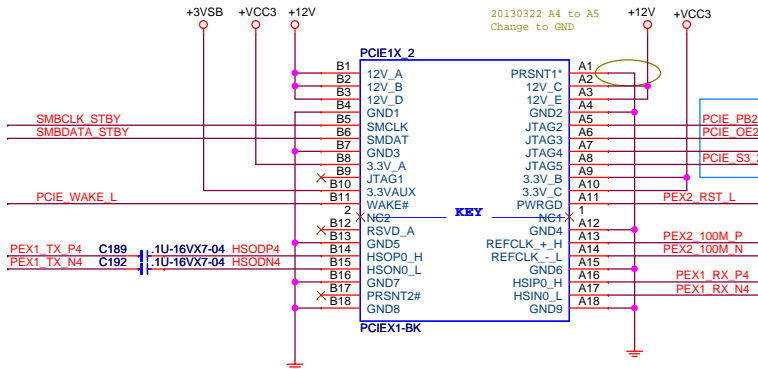
15 PEX1_TX_P5 >> PEX1_TX_P5
15 PEX1_TX_N5 >> PEX1_TX_N5
15 PEX1_RX_P5 >> PEX1_RX_P5
15 PEX1_RX_N5 >> PEX1_RX_N5



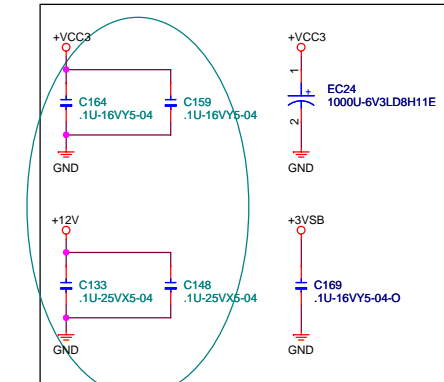
Close PCIE1X 1 Slot



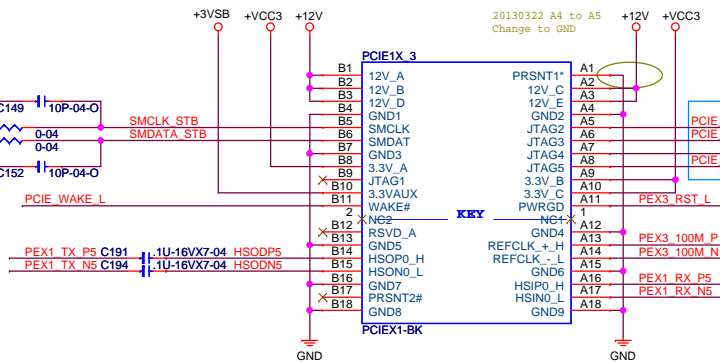
20121107 Pre-A3 to A3
form Reserve to Add
For Lenovo Require



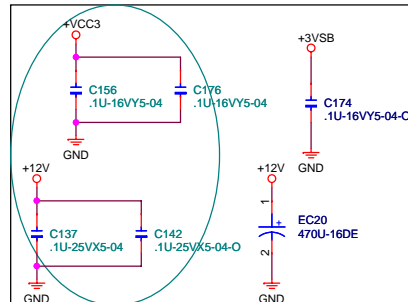
Close PCIE1X 2 Slot



20121107 Pre-A3 to A3
form Reserve to Add
For Lenovo Require



Close PCIE1X 3 Slot



GND C173 1U-16VX7-04-O +VCC3
Stitching cap Reserve

+12V C132 1U-16VY5-04-O GND
Stitching cap Reserve

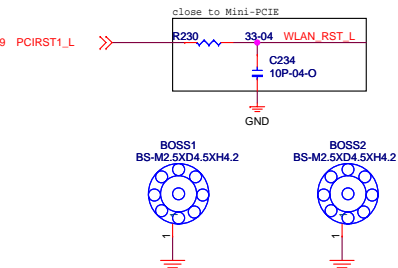
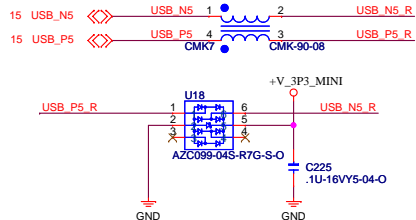
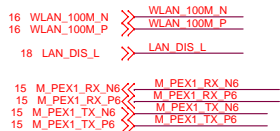
GND C662 1U-16VX7-04-O +VCC
EMI Reserve

20121024 Pre-A3 to A3
For EMI Reserve

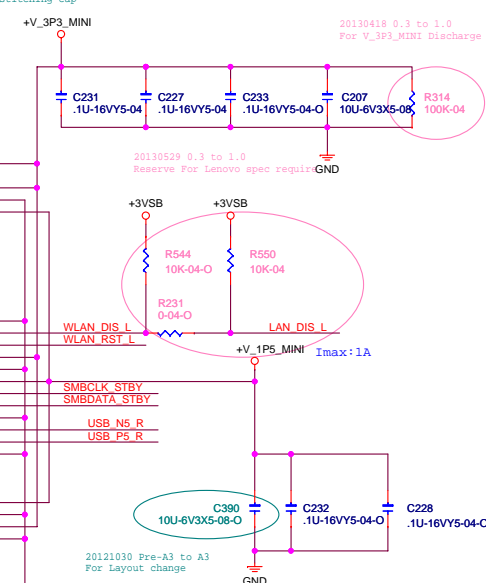
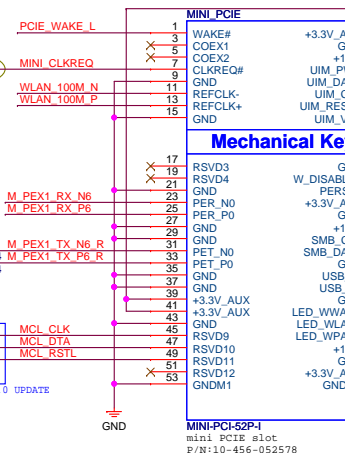
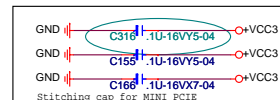
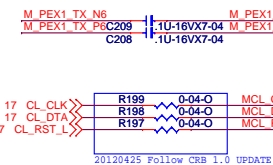
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PCIE1X*3			
Size	Document Number	Rev	
Custom	H81H3-LM	1.0	
Date:	Friday, May 31, 2013	Sheet	21 of 43

MINI_PCIE

20120110 A3 to A4
For Power and PSU Compatibility debug

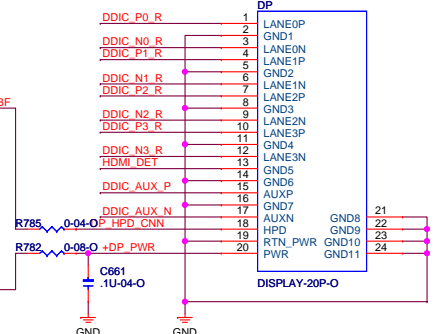
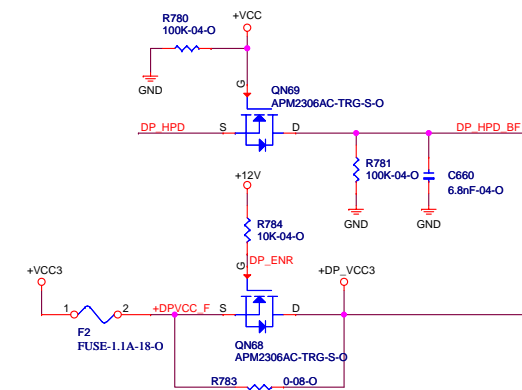
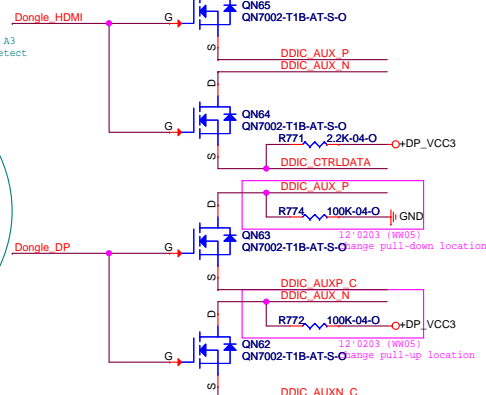
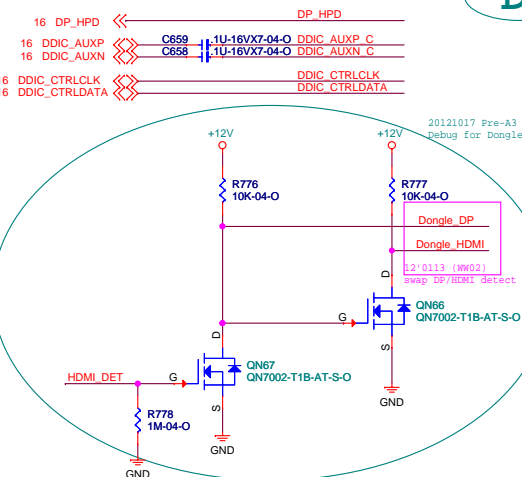


23-765-200745
BOSS.WI-P-G51108A.M2*D4.5*H4.5mm..
CU..SN..HF.LEAD-FREE.GREAT GOLD

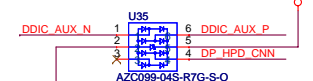
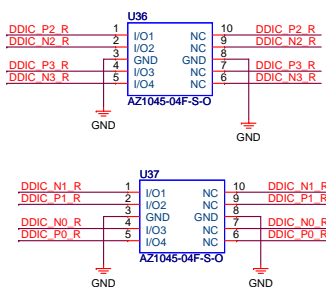
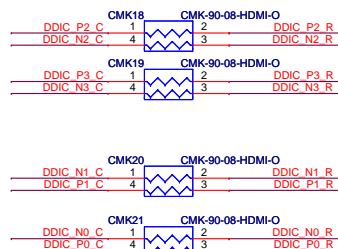
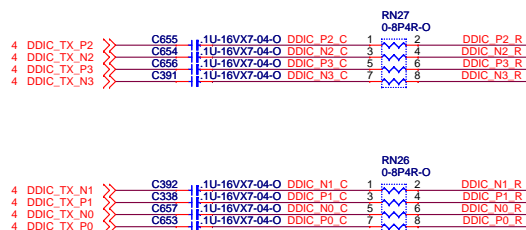


Symbol	Parameter	Min	Max	Units
T _{ACKL}	Power Valid to CLKREQ# Output active		100	µs
T _{INPL}	Power Valid to PERST# Input inactive	1		ms
T _{REFCLK}	REFCLK stable before PERST# inactive	100		µs

DP

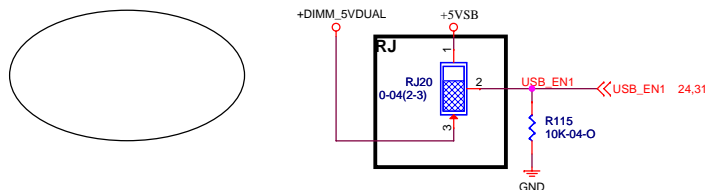
20120911 Pre-A3 to A3
ADD DP function for Lenovo spec

P/N :10-088-020080
CONN.DISPLAY..20P 90D SMD.....30u..W/SCREW
HOLE....3VD51203-M74J-4H...HF.LEAD-FREE.FOXCONN



			
Title			
MINI PCIE/DP			
Size	Document Number		Rev
Custom	H81H3-LM		1.0
Date:	Friday, May 31, 2013	Sheet	22 of 43

	uP7550 Enable use	RJ	S4/S5 USB_5V_DUAL	
*	+DIMM_5VDUAL	0ohm (2-3)	0 Volt	Lenovo S4/S5 w/o USB_5V_DUAL
	5VSB	0ohm (1-2)	5 Volt	

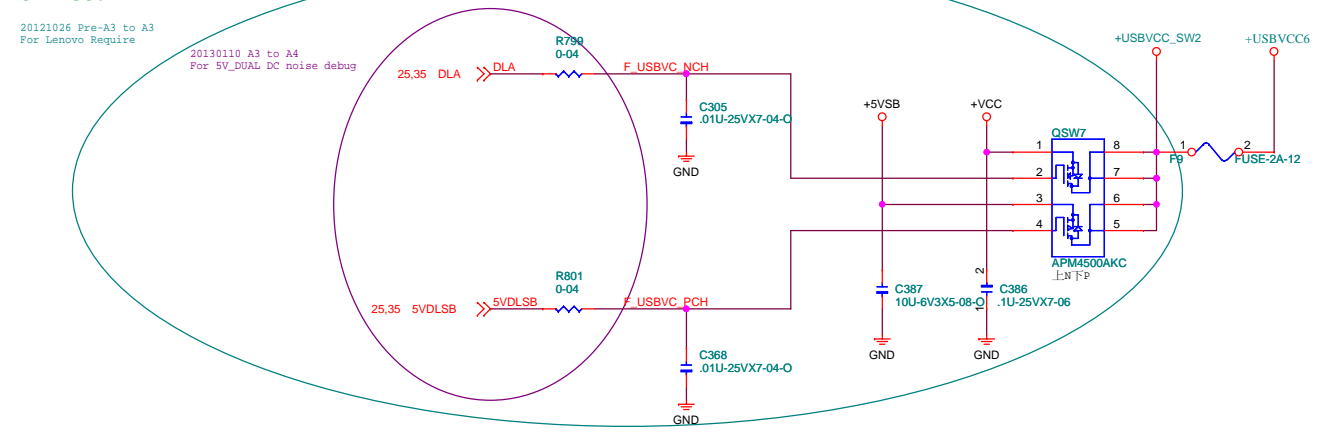


20120810 for Lenovo request

+USBVCC6

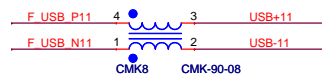
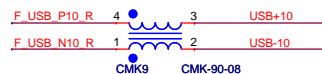
20121026 Pre-A3 to A3
For Lenovo Require

20130110 A3 to A4
For 5V_DUAL DC noise debug

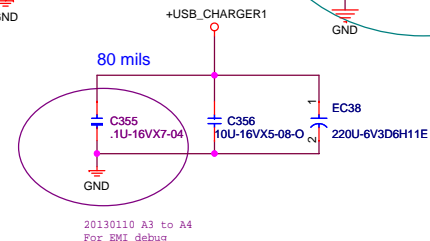
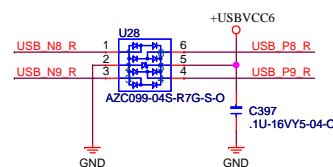
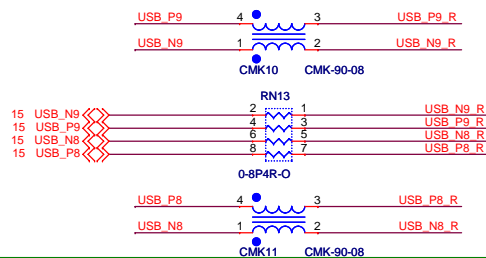
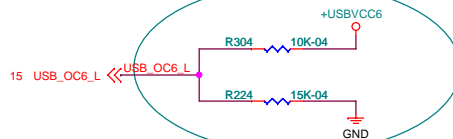


USB2.0 header

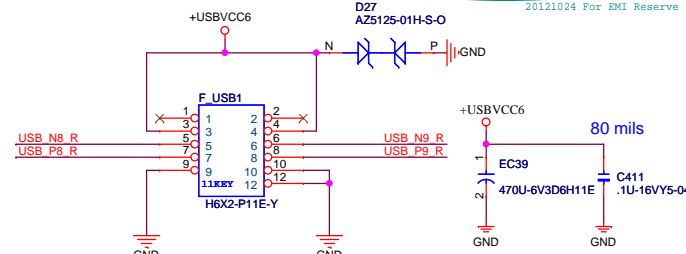
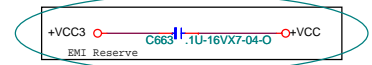
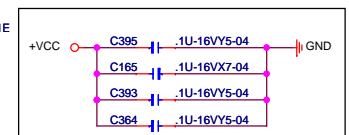
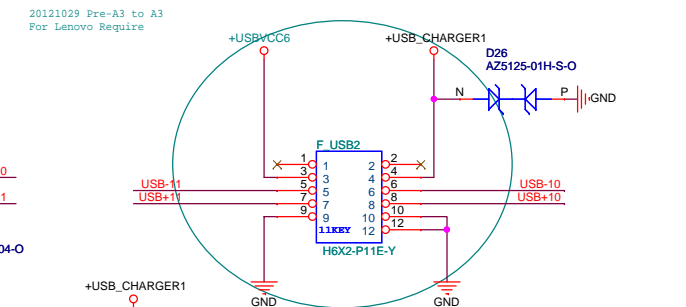
- 25 F_USB_N10_R
- 25 F_USB_P10_R
- 25 F_USB_P11
- 25 F_USB_N11



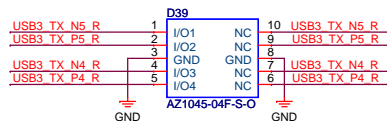
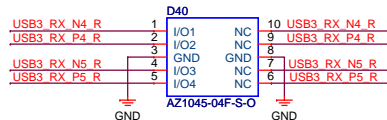
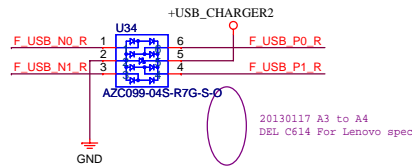
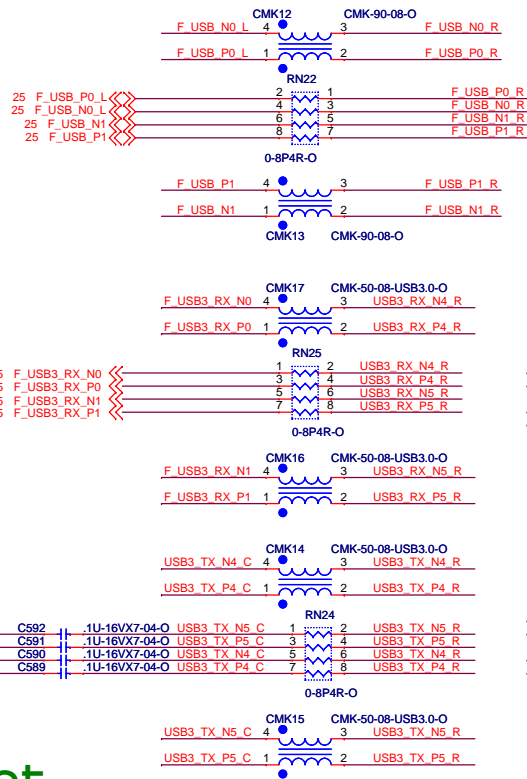
20121029 Pre-A3 to A3
For Lenovo Require



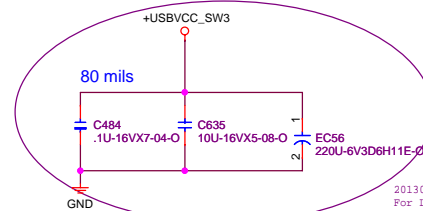
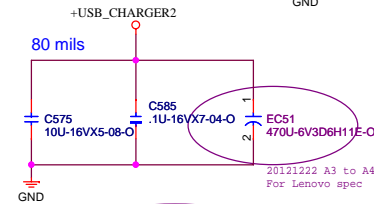
20121029 Pre-A3 to A3
For Lenovo Require



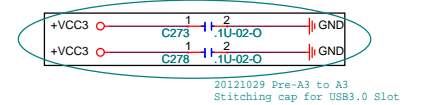
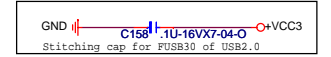
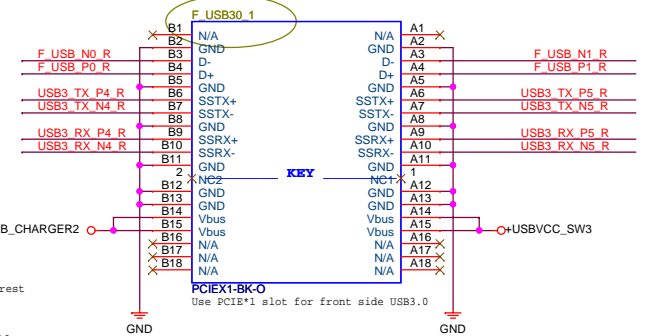
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USB2.0 Header			
Size	Document Number	Rev	
Custm	H81H3-LM	1.0	
Date:	Friday, May 31, 2013	Sheet	23 of 43



20120810 for Lenovo requirement

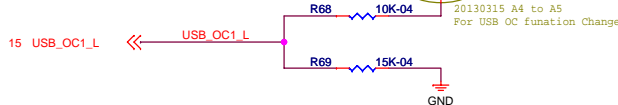
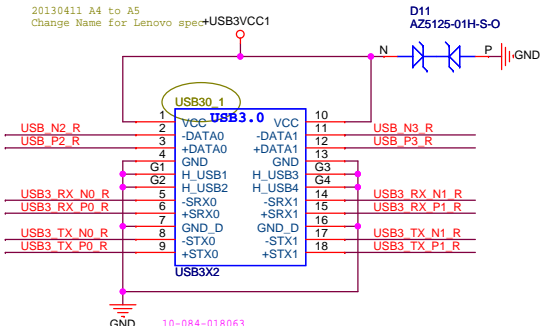
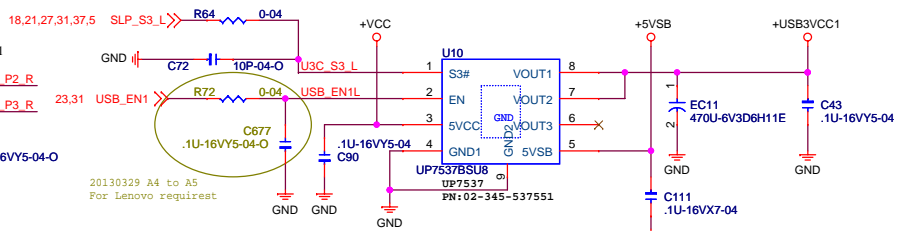
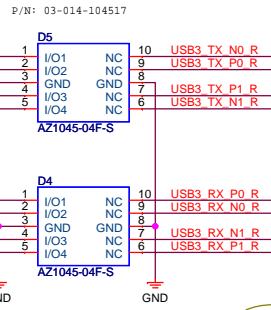
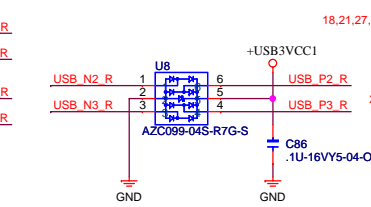
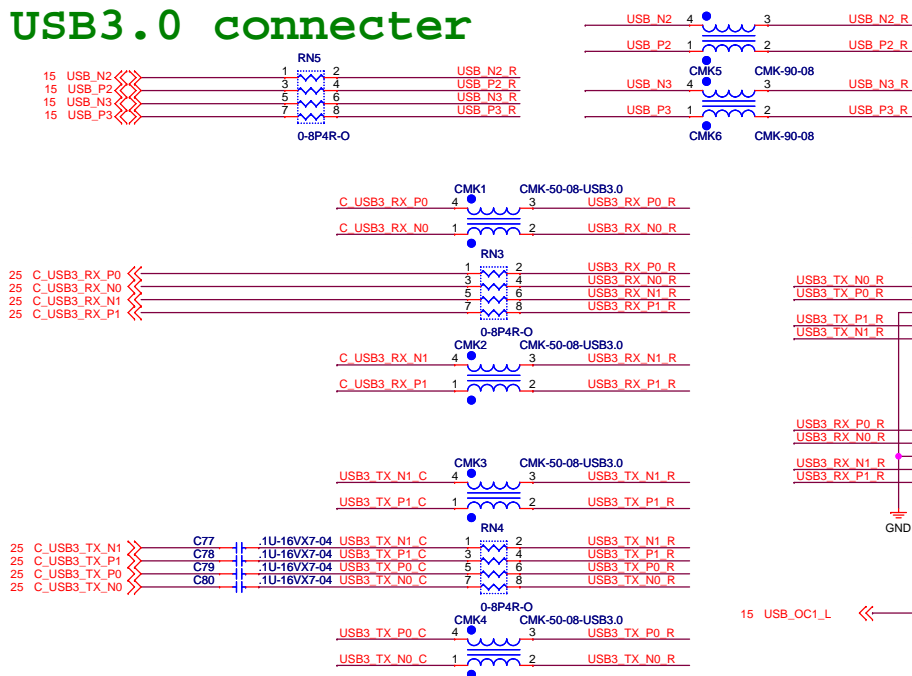


20130411 A4 to A5
Change Name for Lenovo spec

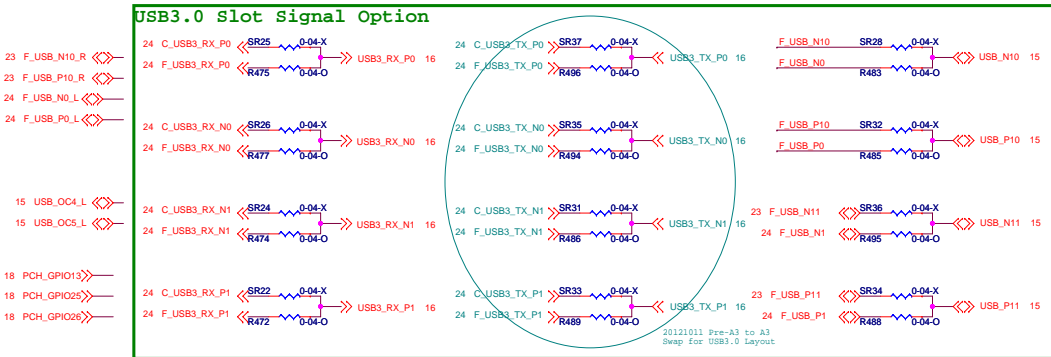
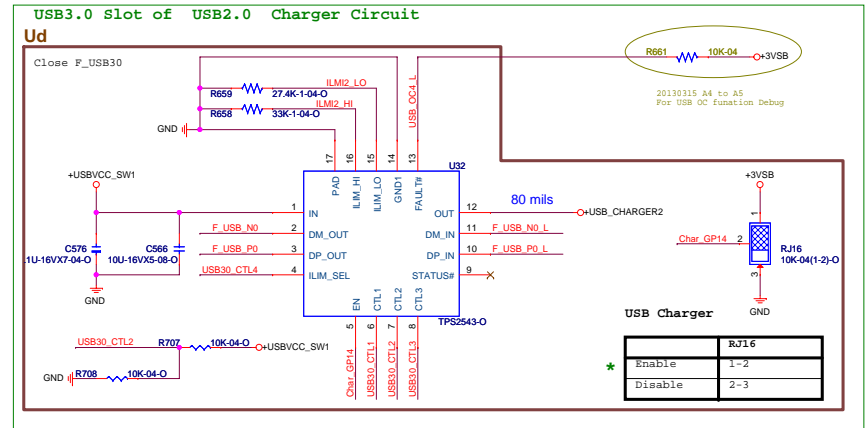
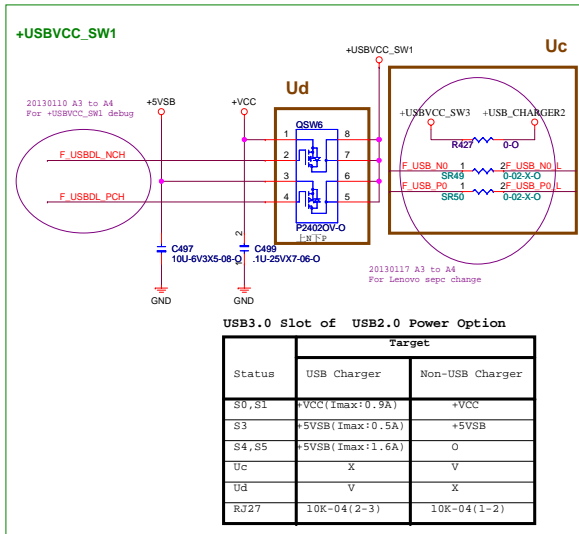
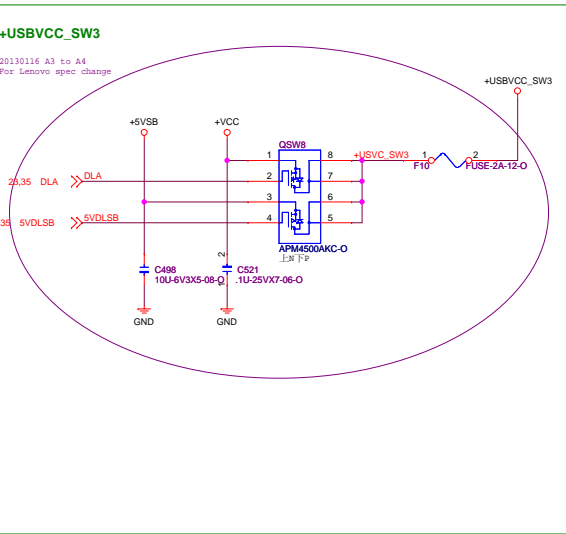
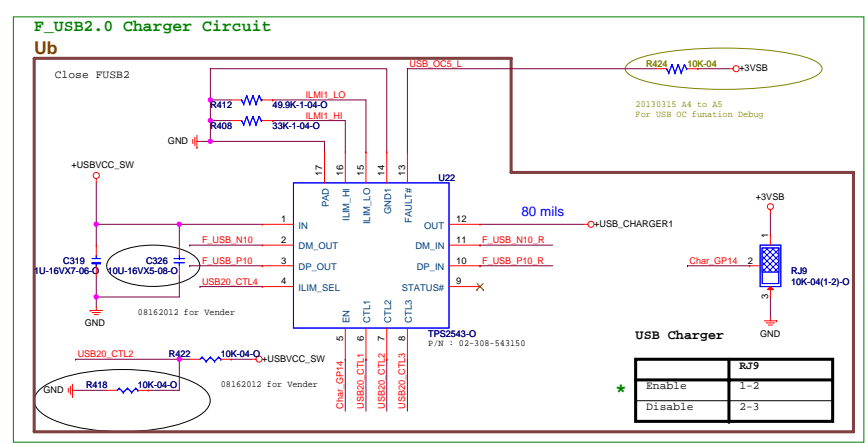
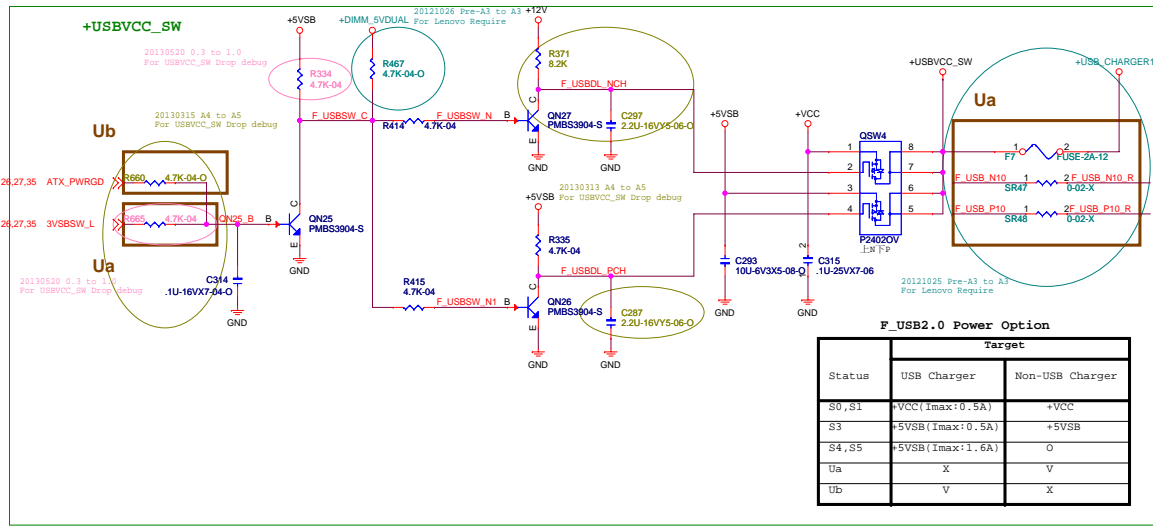


USB3.0 slot

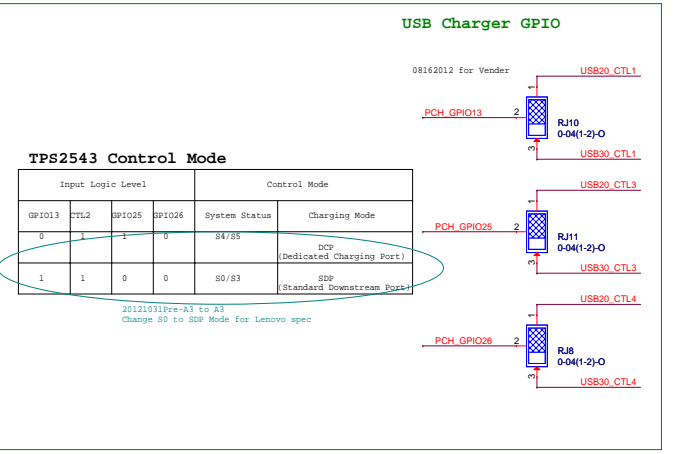
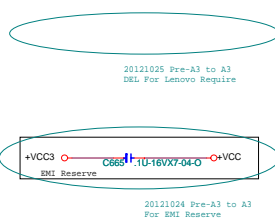
USB3.0 connector

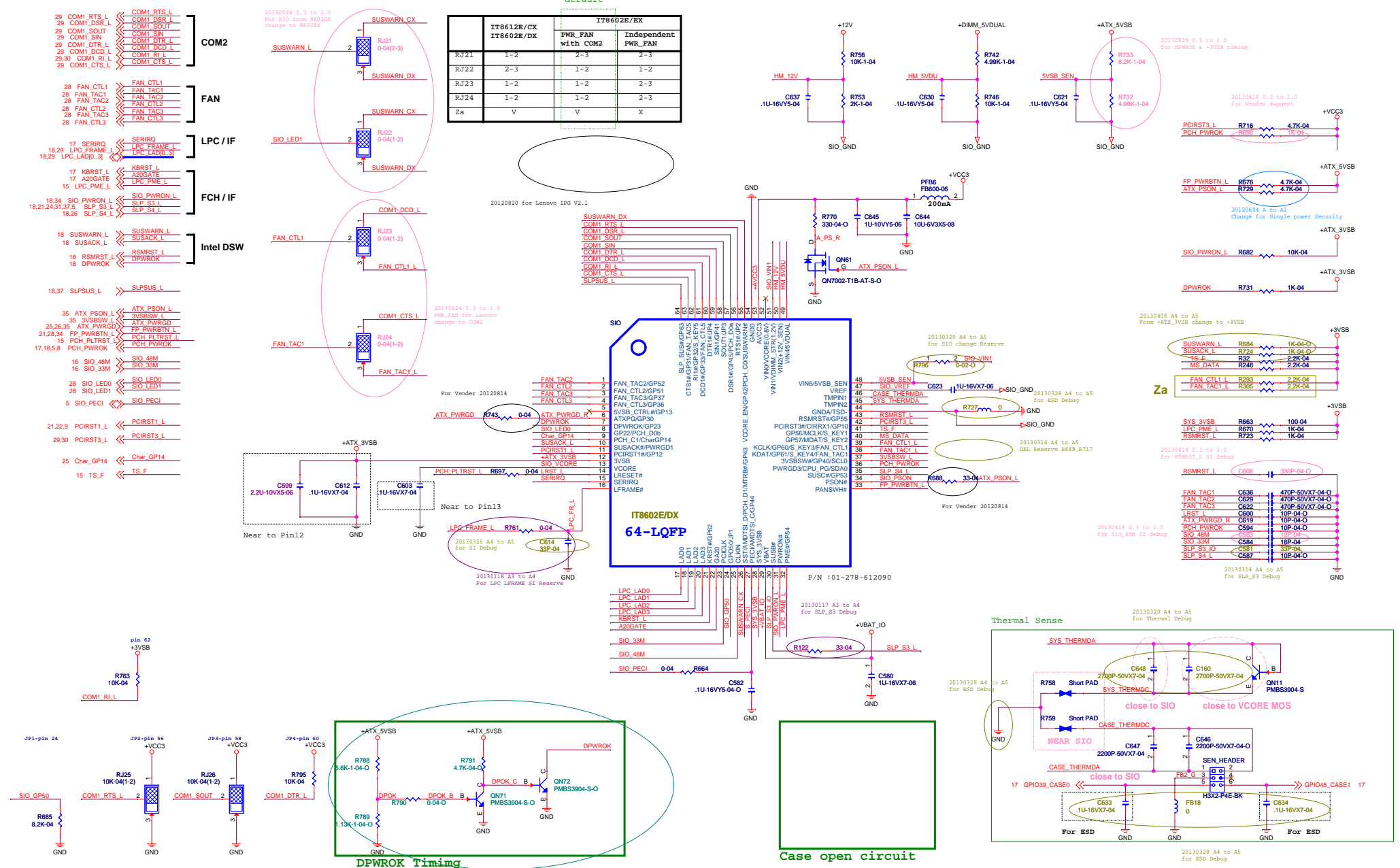


Title			
USB3.0 Conn & Slot			
Size	Document Number	Rev	
Custom	H81H3-LM	1.0	
Date:	Friday, May 31, 2013	Sheet	24 of 43



USB Charger Power-On Reset





Symbol	Value	Description
JP1	DSW_EUP_SEL	1
Pin-24	0 *	DSW
JP2	WDT_EN	1 *
Pin-56	0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1 *
Pin-58	0	EC Index 63h/6Bh/73h is 80h
JP4	K8PWR_EN	1 *
Pin-60	0	Disable K8 Power Sequence

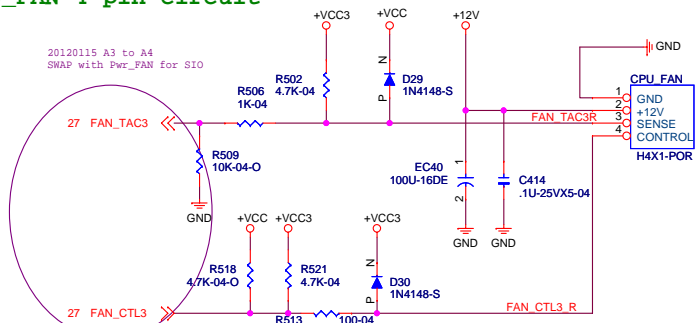
Note: If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

NOTE:

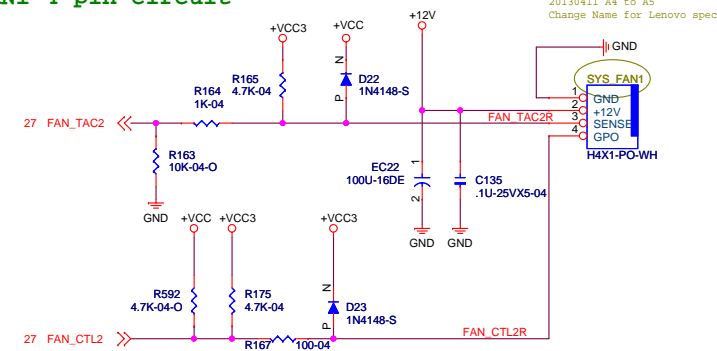
If without use these pins, Please pull-up. Don't let it floating.

Pin:6/24/28/30/33/35/38-41/50/56/58/60

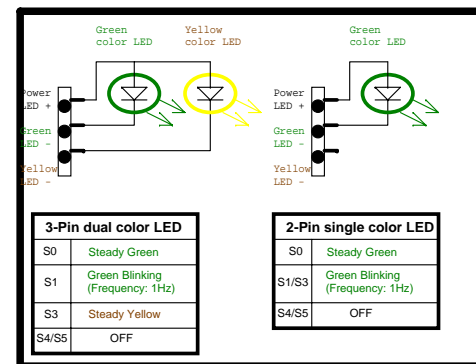
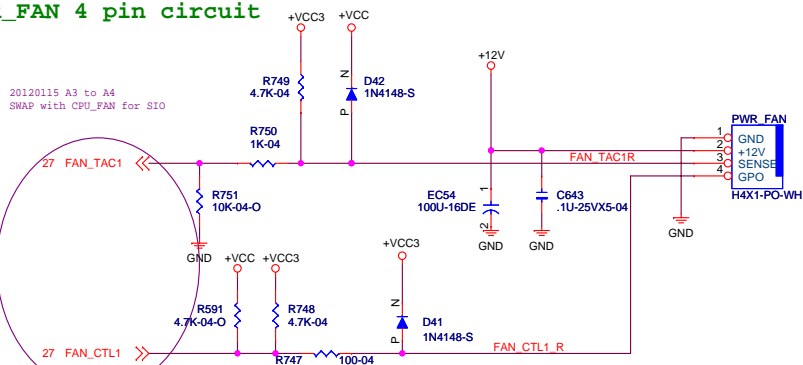
CPU_FAN 4 pin circuit



SYS_FAN1 4 pin circuit



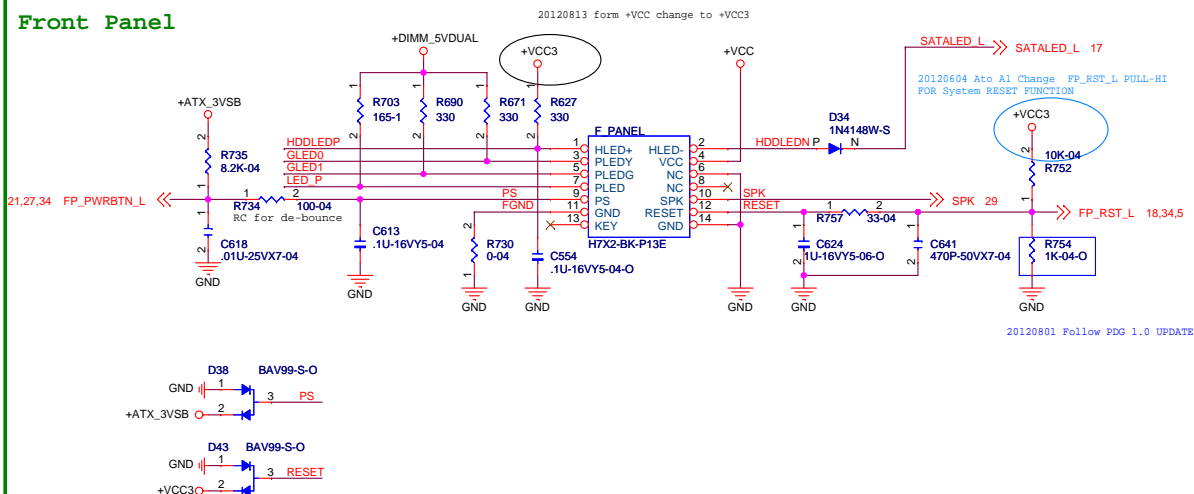
PWR_FAN 4 pin circuit



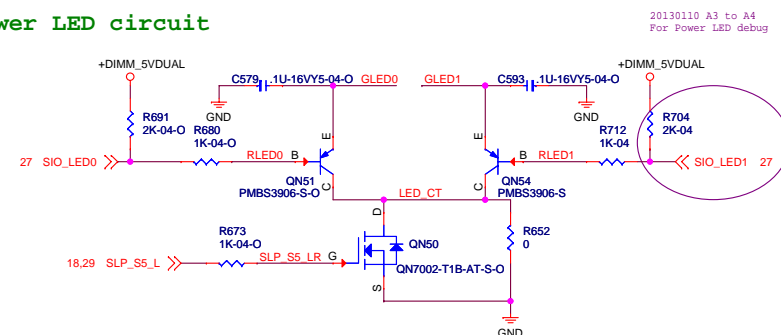
Lenovo LED線路阻値330-06

Source Voltage (V)	5
LED Forward Voltage (V)	1.8
BIT Vce(s) (V)	0
Pull Up Resistor (ohm)	330
LED Forward Current (A)	0.009697
Pull Up Resistor Power (R<1/10 W)	0.03103
LED Power (W)	0.017455

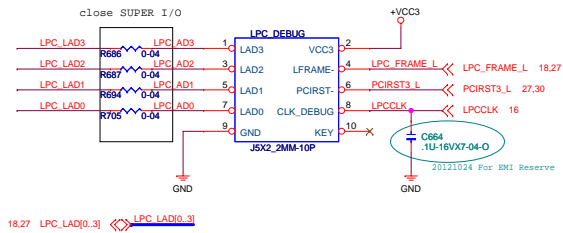
Front Panel



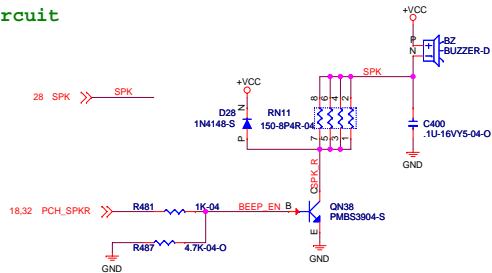
Power LED circuit



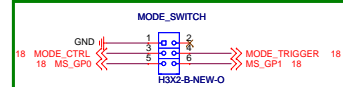
LPC_DEBUG Header Circuit



Buzzer circuit



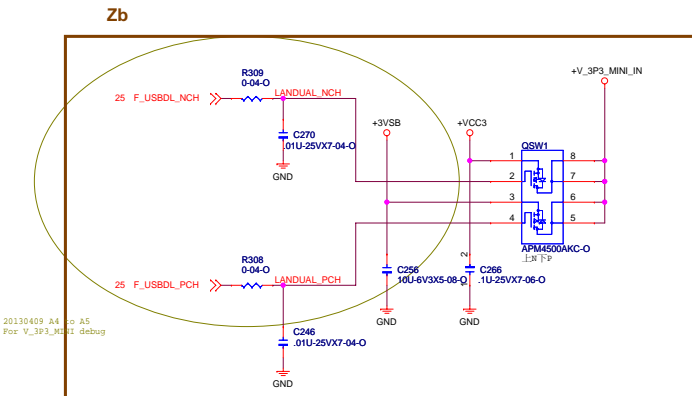
MODE_SWITCH Header



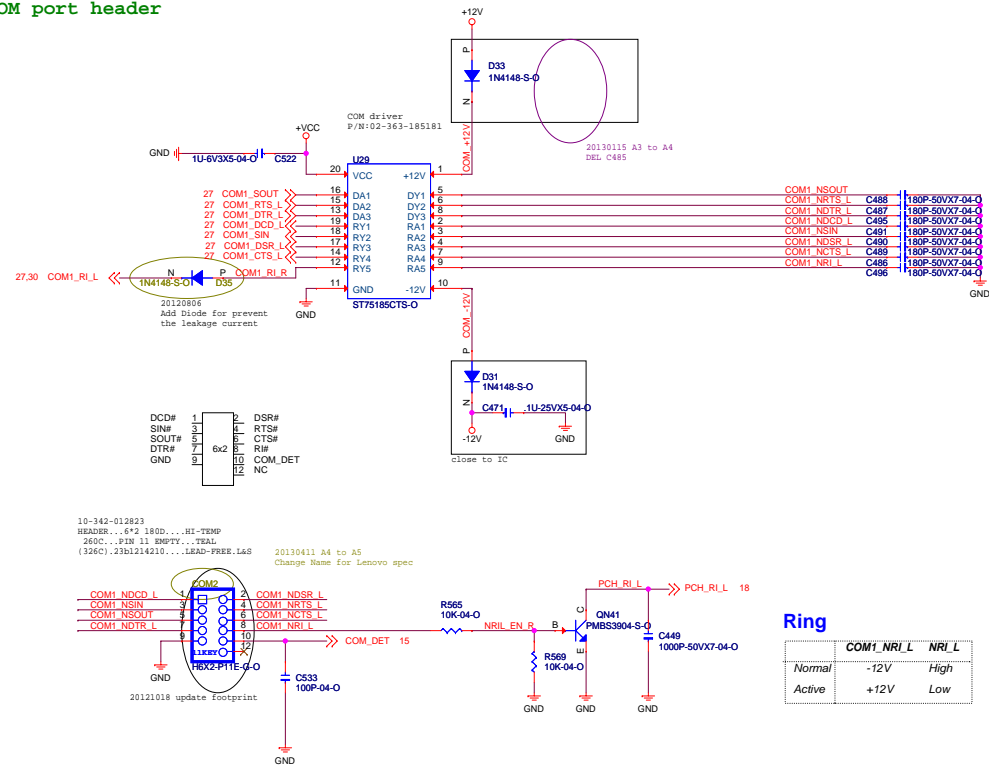
Close COM port Header

+V_3P3_MINI

Note : Wake Up Operation Mode : S3, S4



COM port header

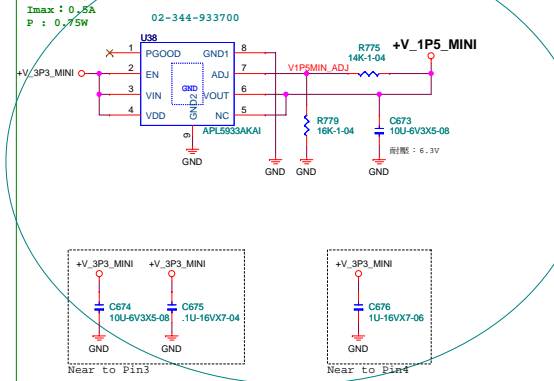


Ring

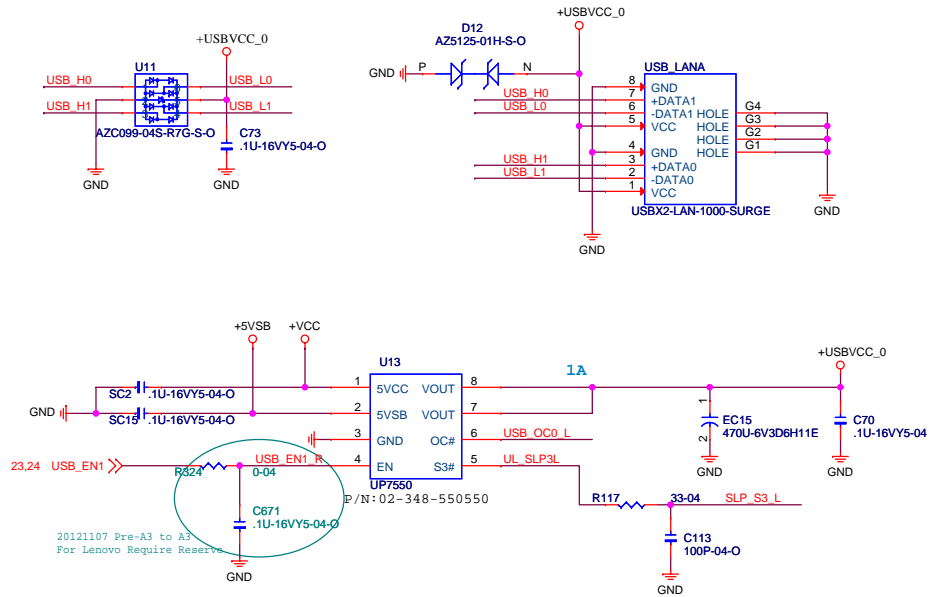
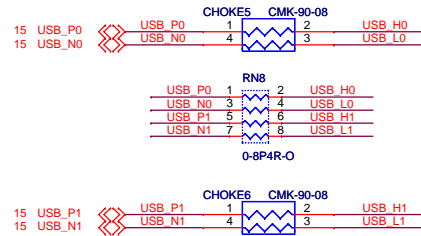
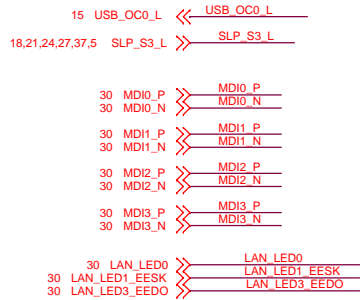
	COM1_NRI_L	NRI_
Normal	-12V	High
Active	+12V	Low

+V_1P5_MINI

Vout : 1.5V



	+V_3P3_MINI Power	
Status	USB Charger	Non-USB Charger
Za	0(1-2)	0(2-3)
Zb	V	X



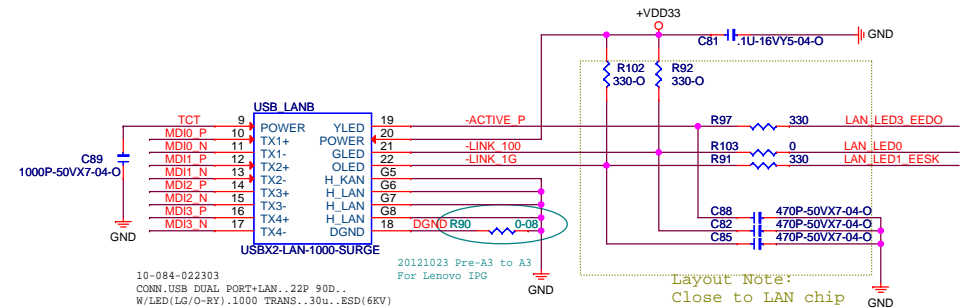
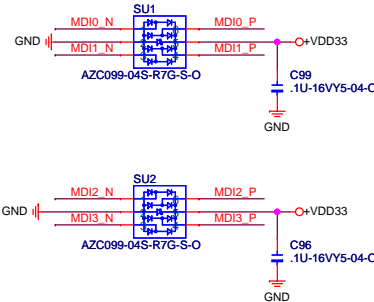
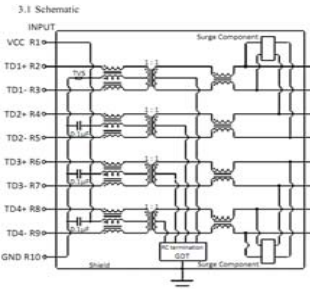
WOL	status	Yellow	Grn/Org
don't care	No Link	off	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off	off
on	10M.inactive	off	off
on	10M.active	off	off
on	100M.inactive	off	off
on	100M.active	off	off
on	1G.inactive	off	off
on	1G.active	off	off

always on

always on

always on

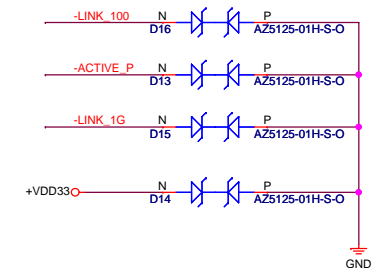
blinking



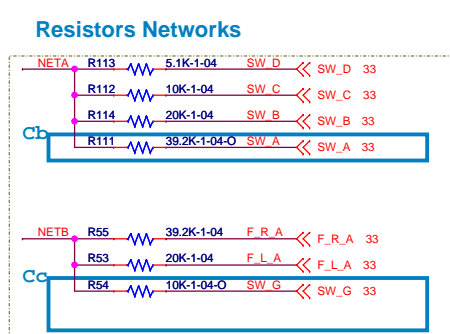
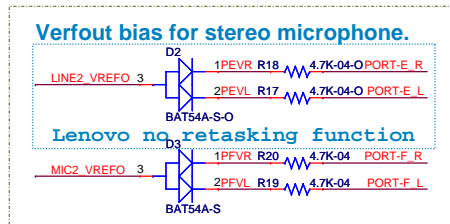
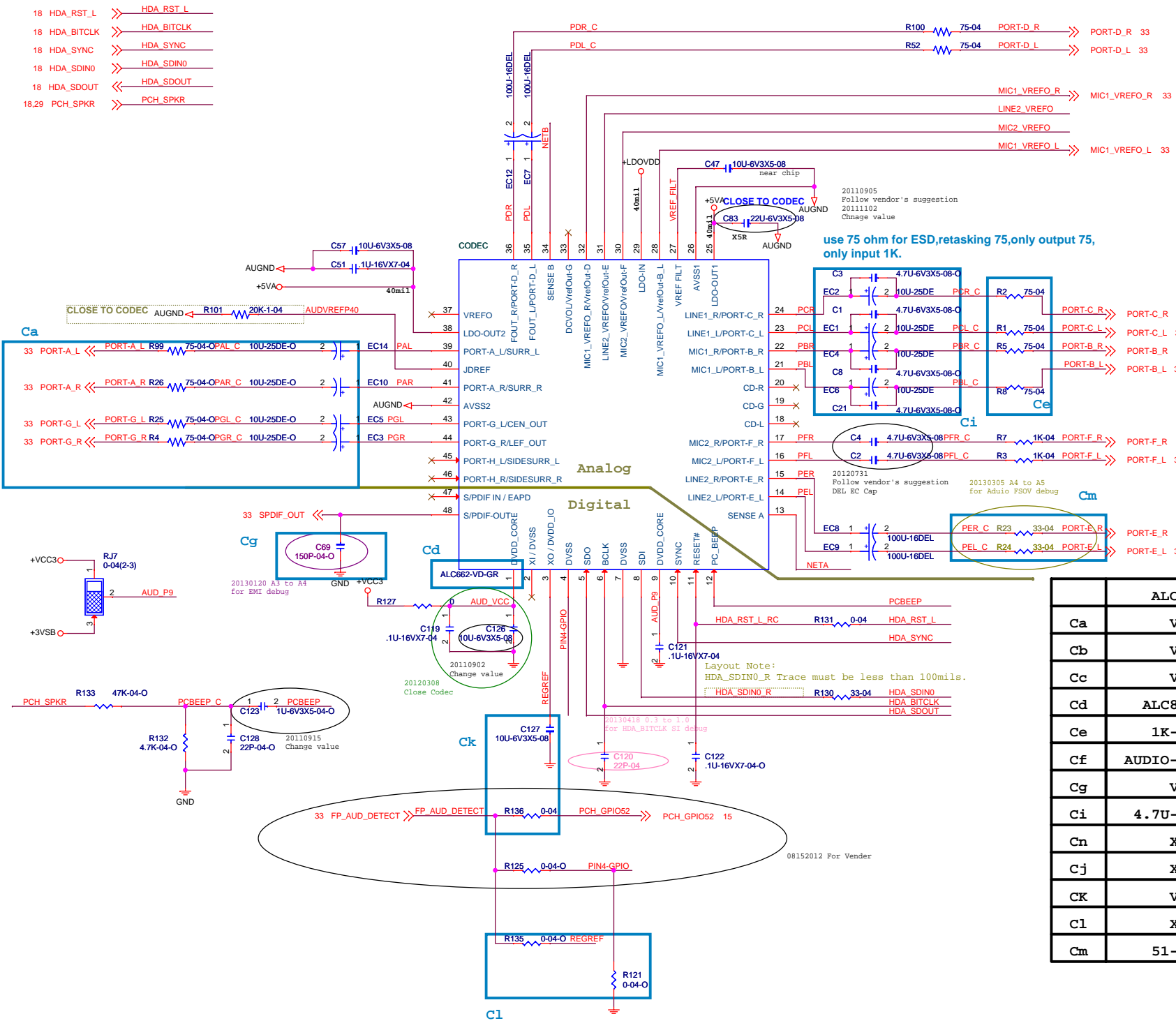
Place Caps in Bottom Side.

MDIO_P SC4	2.7P-04-X-O
MDIO_N SC1	2.7P-04-X-O
MDI1_P SC5	2.7P-04-X-O
MDI1_N SC3	2.7P-04-X-O
MDI2_P SC16	2.7P-04-X-O
MDI2_N SC14	2.7P-04-X-O
MDI3_P SC18	2.7P-04-X-O
MDI3_N SC17	2.7P-04-X-O

EMI value must be tuned

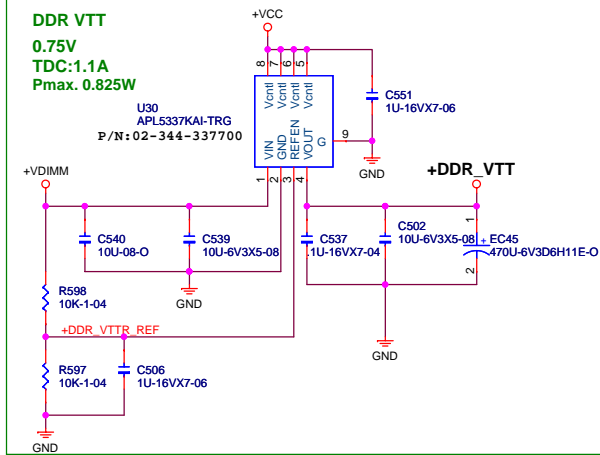


Title			
LANUSB CONN			
Size	Document Number	Rev	
Custom	H81H3-LM	1.0	
Date:	Friday, May 31, 2013	Sheet	31 of 43



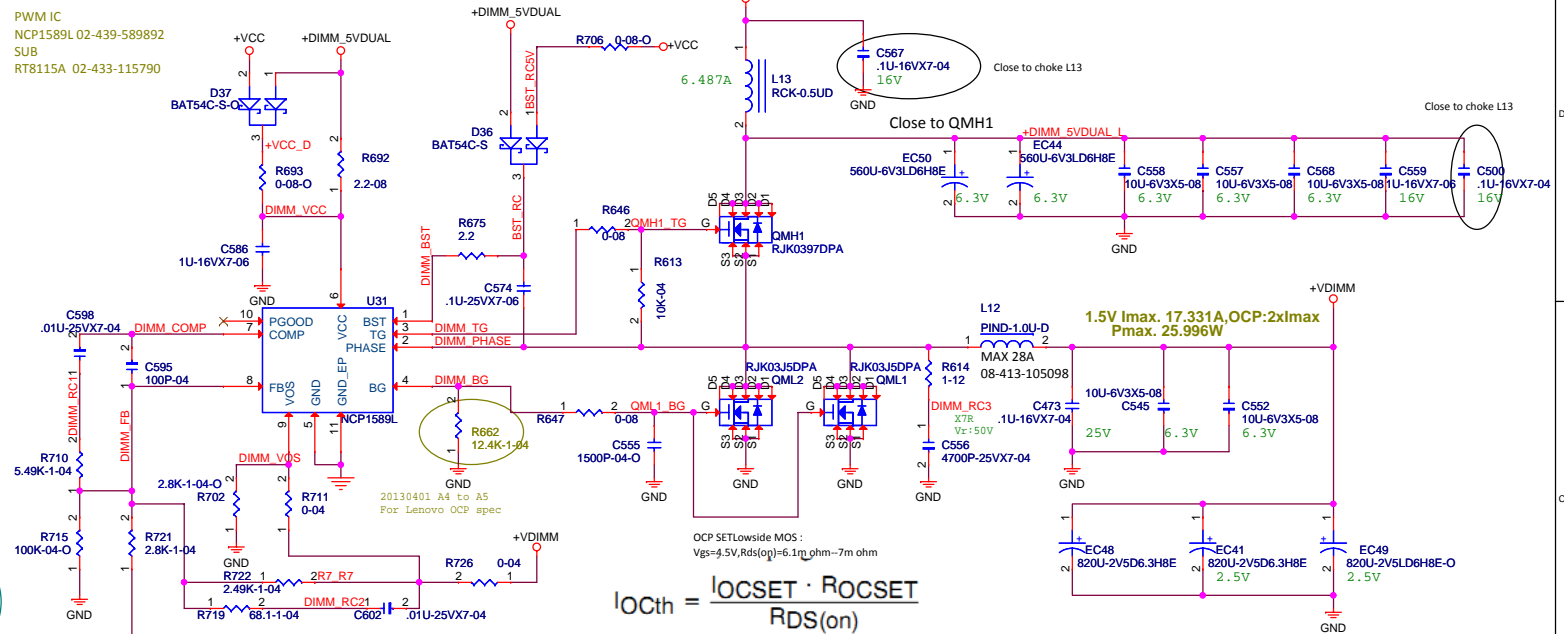
	ALC892	ALC662-VC	ALC662-VD
Ca	V	X	X
Cb	V	X	X
Cc	V	X	X
Cd	ALC892-CGS	ALC662-VC-GR	ALC662-VD-GR
Ce	1K-04	75-04	75-04
Cf	AUDIO-25P	AU-13P-BL+LI+PK	AU-13P-BL+LI+PK
Cg	V	X	X
Ci	4.7U-X5-09	10U-25D4H5E	10U-25D4H5E
Cn	X	V	V
Cj	X	V	X
CK	V	X	V
Cl	X	V	X
Cm	51-04	33-04	33-04

DDR VTT 0.75V TDC:1.1A Pmax. 0.825W



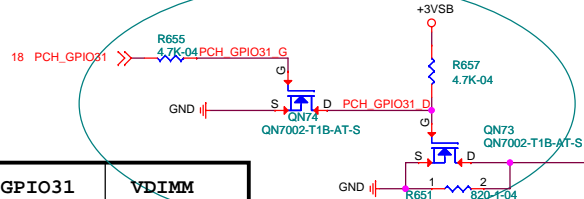
DDR3 POWER

PWM IC
NCP1589L 02-439-589892
SUB
RT8115A 02-433-115790



$$I_{Oth} = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{DS(on)}}$$

PWM IC
NCP1589L
MOSFET:
RJK03J5DPA+RJK03J5DPA
NTMFS4927+NTMFS4925
SM4365NAKPC+SM4364NAKPC

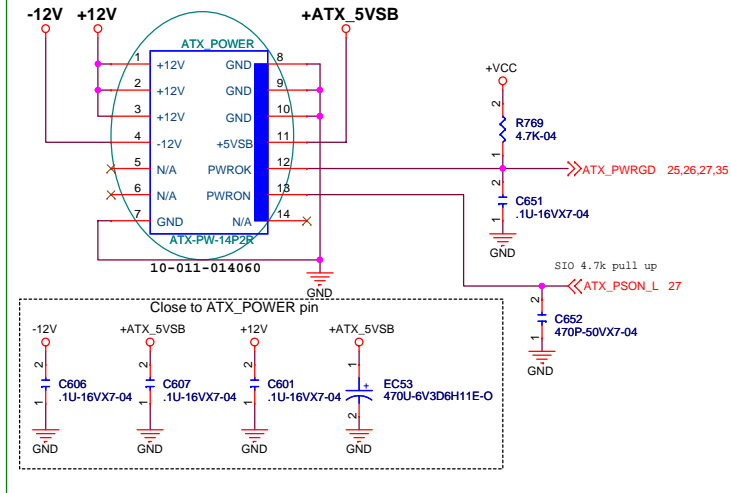


GPIO31	VDIMM
L	1.5V
H	1.35V

* GPIO31 with internal pull-down

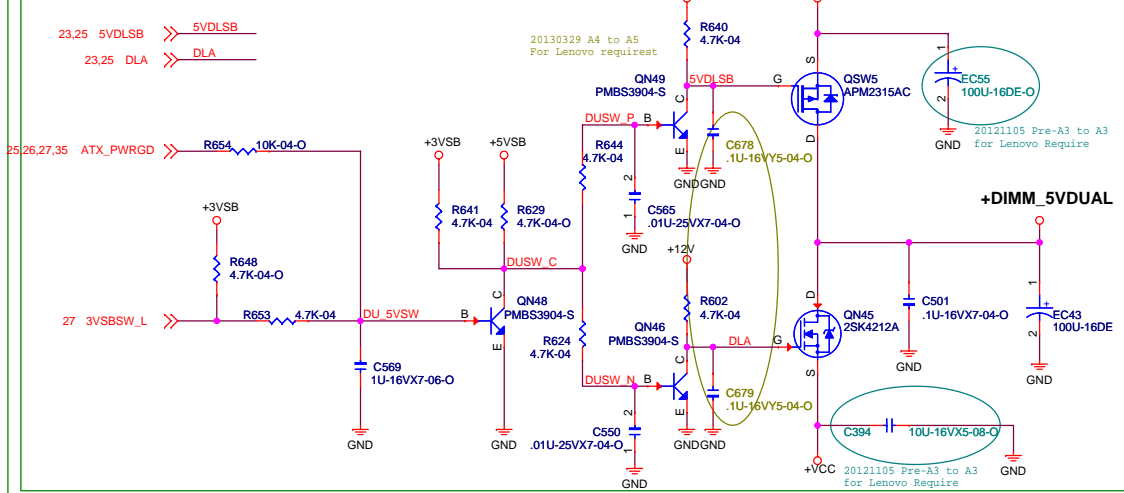
ATX Power Connector

20120820 Pre-A3 to A3
Change footprint for Lenovo IPG V2.1

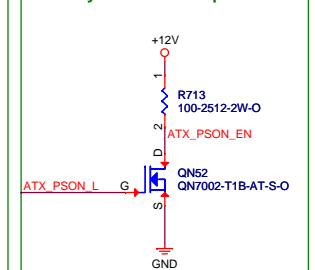


5VDUAL I_{max}. 6.487A

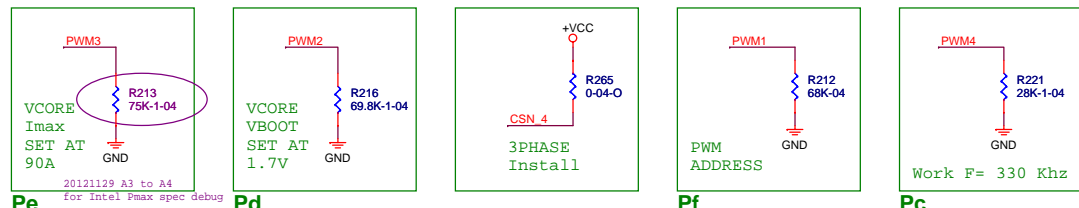
23,25 5VDLSB >> 5VDLSB
23,25 DLA >> DLA



Dummy Load for ATX power

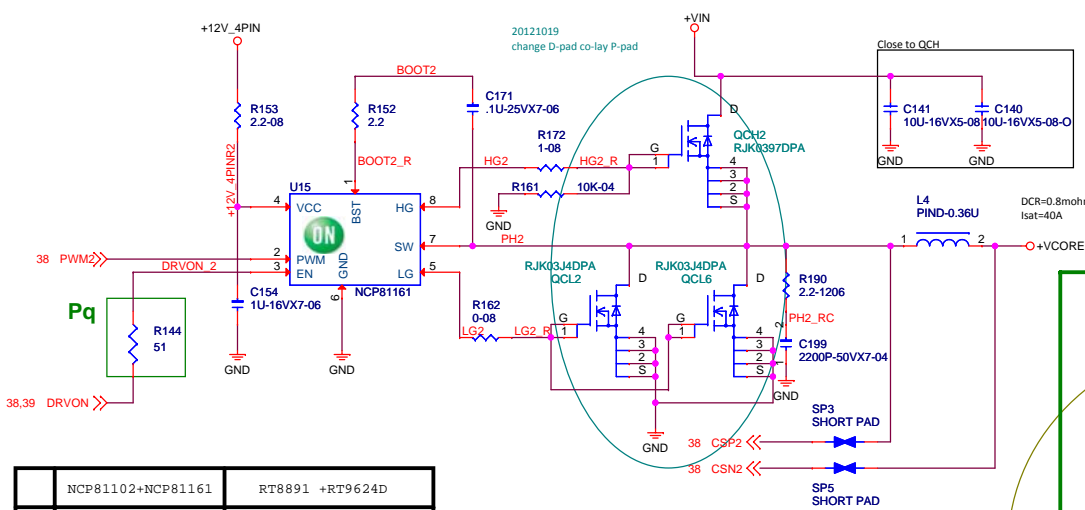
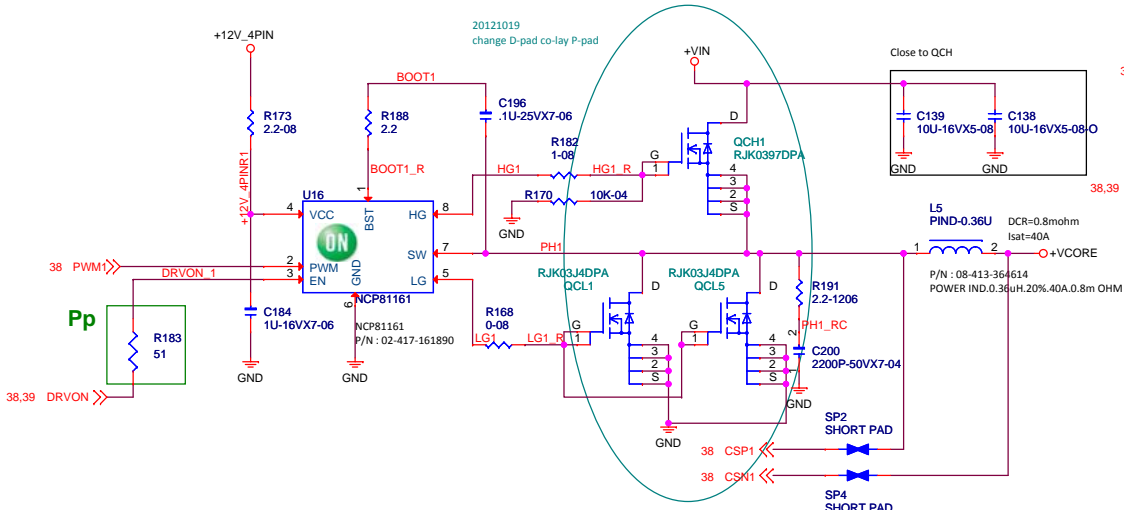
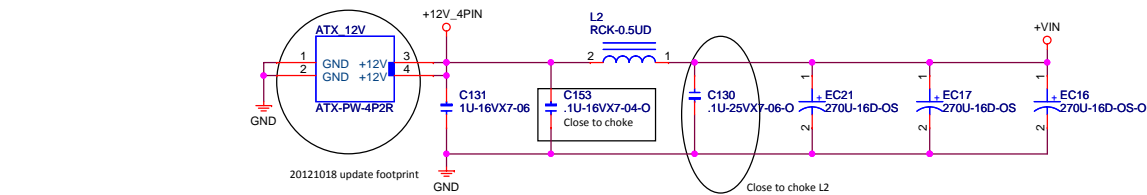


20121129 A3 to A4
for Intel Pmax spec debug

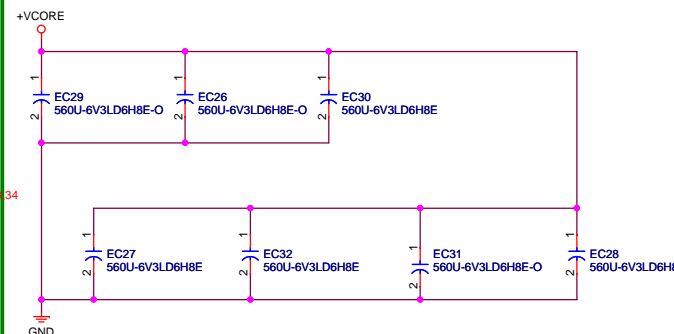
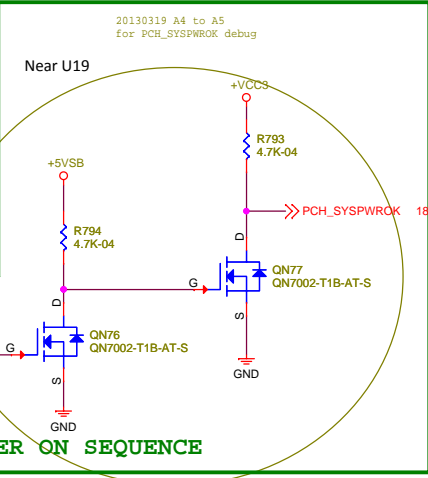
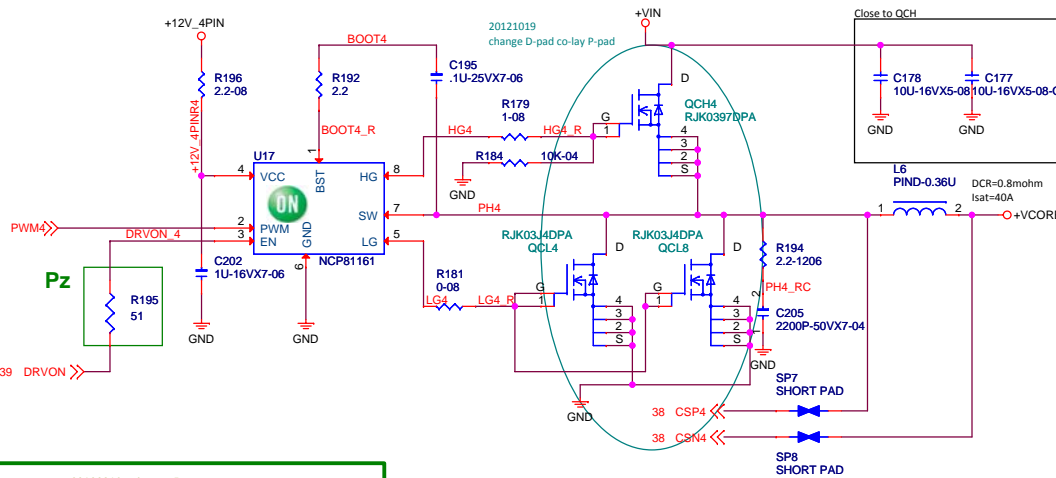
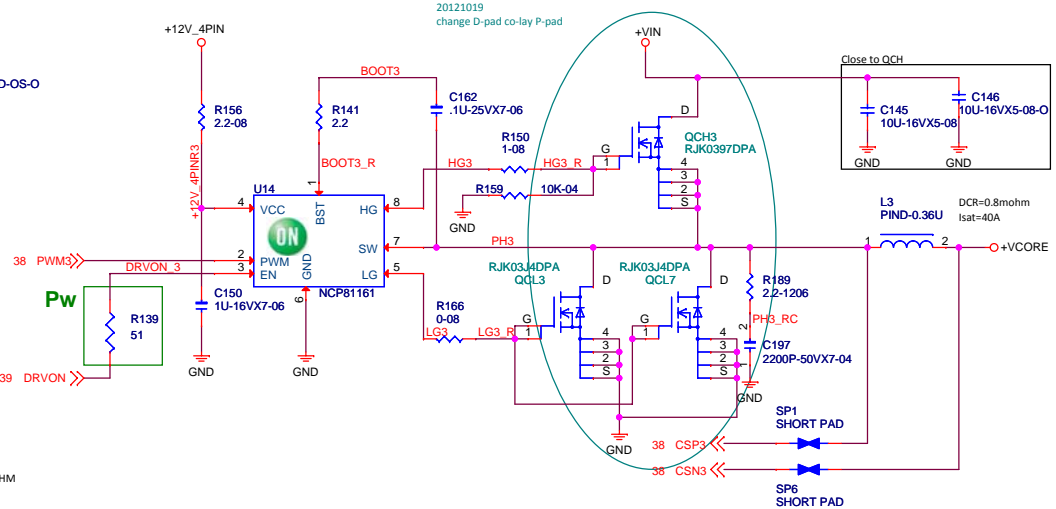


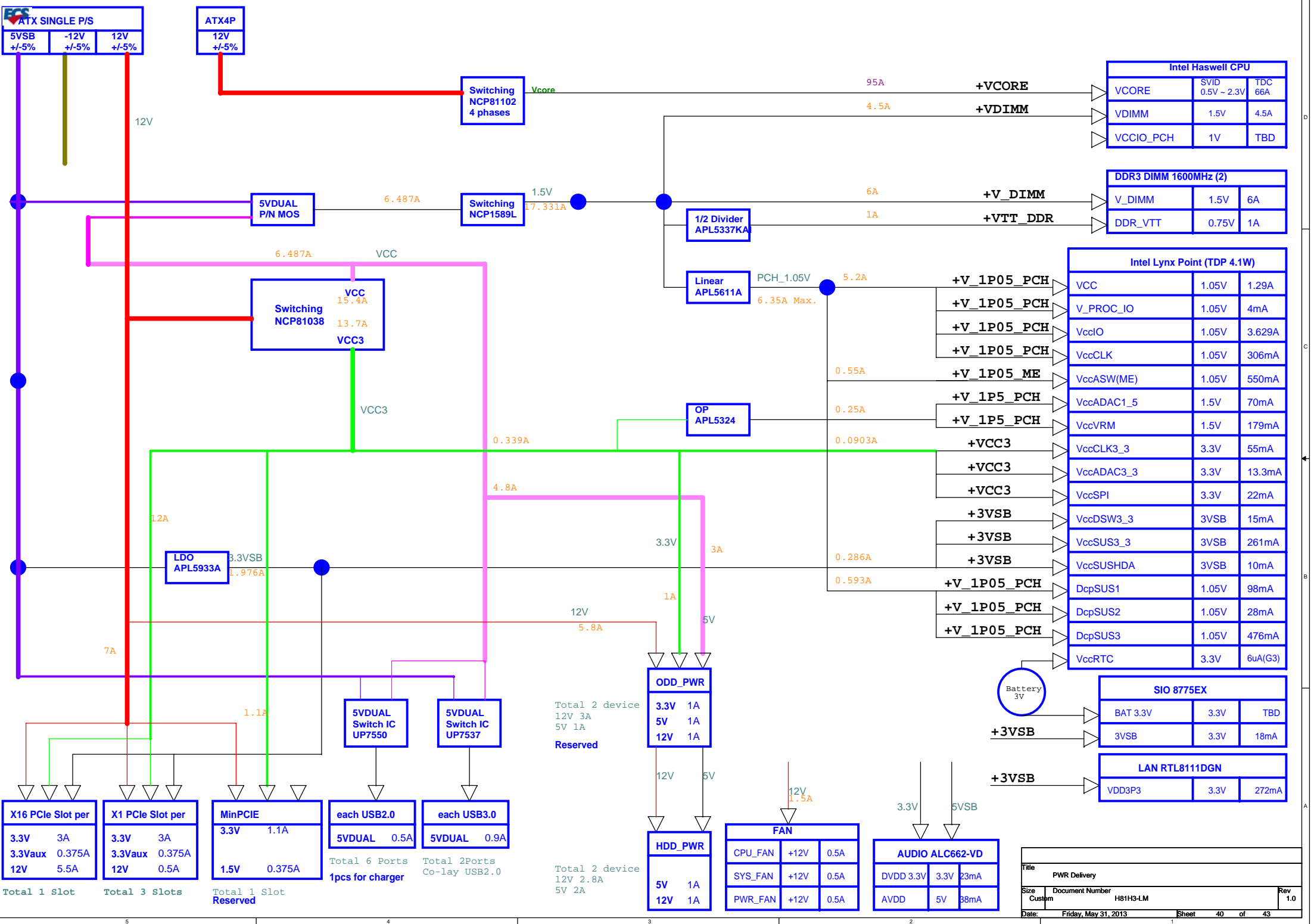
The SVID interface provides the platform ICC_MAX value at register 21h for. A resistor to ground on the IMAX pin programs these registers at the time the part is enabled. 10uA is sourced from these pins to generate a voltage on the program resistor. The value of the register is 1A per LSB and is set by the equation below. The resistor value should be no less than 10k.

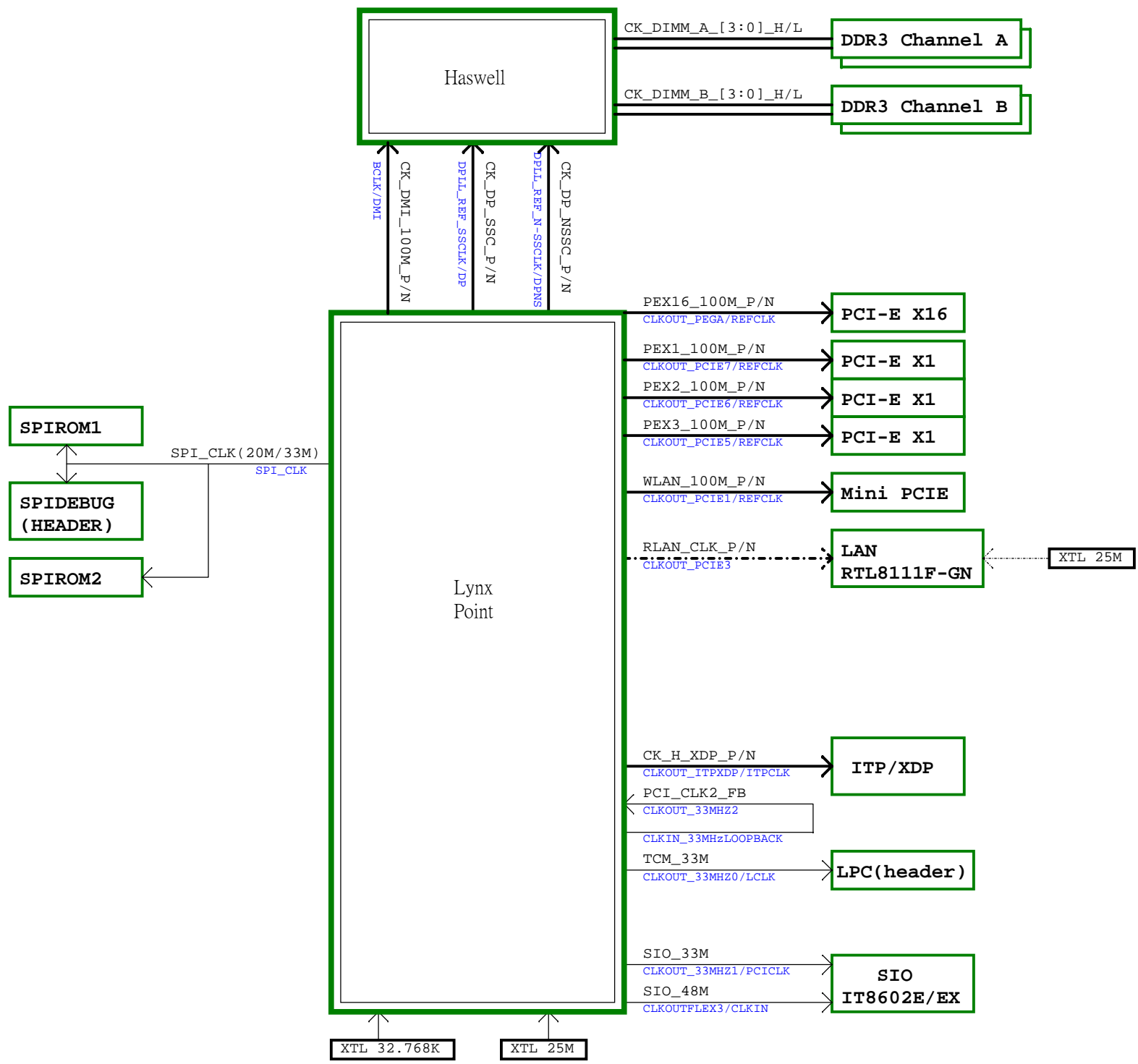
$$ICC_MAX_{21h} = \frac{R * 10\mu A * 256A}{2V}$$



	NCP81102+NCP81161	RT8891 +RT9624D
Pq	V	X
Pp	V	X
Pw	V	X
Pz	V	X







REVISION HISTORY:


Rev	Date	Notes
A2	2012/08/16	From H81H3-LM V:A

Rev	Date	Notes
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A3	2012/09/30	1. U33 From APL5932AKAI Change to APL5933AKAI for Vender Process 2. DP Dongle Detect circuit form +VCC change to +12V 3. QN66,QN67 from 3904 chage to 2N7002 For Dongle Detect debug 4. R348 Resrve for Intel no Overclocking function 5. Del HSW Strap CFG13 circut H81 no Overclocking function 6. R272 Change Vaule for Load Line debug 7. R284 Change Vaule for lout Debug 8. USB3.0 TX Signal Option Swap for Layout 9. ATX_POWER change footprint for Lenovo IPG V2.1 spec 10. ME_DIS control circuit reserve For Lenovo Require 11. RJ16 DEL for BOM detect is enough 12. ADD R530,R660,R661 For USB OC function Debug 13. ADD R406 for reboot Issue from Intel WW39 14. TPS2543 Control Mode chahge for Lenovo spec 15. Vore option Table(RT8891+RT9624D) change Vaule for test debug 16. ADD DP function for Lenovo spec 17. ADD DPWROK cirtcuit for Intel Timimg(Deep Sx to G3) 18. QCH1,QCH2,QCH3,QCH4,QCL1,QCL2,QCL3,QCL4,QCL5,QCL6,QCL7,QCL8 change D-pad co-lay P-pad for Lenovo require 19. Reserve C316 for MIN_PCIE USB signal stitching cap 20. R90 Change 0603 to 0805 for Lenovo IPG 21. Y HOLDER1 change to Iron wire for Lenovo require 22. Reserve C662,C663,C664,C665 for EMI debug 23. R409,R327 from 21K change 18K to for +VCC&VCC3 OCP debug 24. DEL USB Charger Power-On Reset circuit for Lenovo require 25. Update USB Charger circuit for Lenovo require 26. DEL R224 for USB OC_3 debug 27. Power circuit(+USBVCC6) from UP7550 change to DUAL MOS(APM4500AKC) for Lenovo require 28. F_USB2 USB port(USB +/-10) power from +USB_CHARGER1 change to +USBVCC6 29.Reserve Stitching cap C273,C278 for USB3.0 Slot 30.F_USB2 of USB port 10 and 11 SWAP for Lenovo require 31.PCIE WAKE Mode change for WOL G3 to S5 function 32.ADD R444,R453 For Intel +V_1P05_PCH&+VCC3 Power sequence 33. DEL EC34, ADD C390 for layout space 34. C670,C666,C693,C672,C668,C667 Reserve for SPI Debug 35. DEL PCH XDP Header for Lenovo Require 36. Reserve C394 for +DIMM_5VDUAL noise debug Lenovo Require 37. Reserve EC55 for +5VSB noise debug Lenovo Require 38. Reserve C669 for 48M Clock debug 39. ADD R324,C671 to USB_EN1 delay for Lenovo Require 40. QN9,QN10,QN39,QN55,QN32 from 3490 change to 2N7002 for Lenovo Require 41. ADD +VDIMM circuit(1.5V coly-lay 1.35V) for Lenovo Require 42. +V_1P5_MINI power circuit change to LDO for Lenovo Require 43. ADD F3 for +VDD3 timing spec 44. ADD QN78,Q2 for OBFF debug
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Rev	Date	Notes
0.2	2013/01/18	1 .SIO form IT8775EX change to IT8612E/CX co-lay IT8612E/DX for spec change 2. DEL SSD_PWR circuit for spec change 3. Resrve R72 follow CRB 4. DEL C16,C14,C15 for VGA Rise and Fail time debug 5. C25,C26,C27 change to 10pF for VGA Rise and Fail time debug 6. R79 change to 3K,ADD RJ6(1-2),RJ4(1-2) For HDMI Debug 7. DEL SPIROM2 circuit for Lenovo Spec change 8. DEL Case Open circuit for Lenovo Spec change 9. USB_OC3_L pull-high change to +3VSB For MINI_PCIE Compatibility debug 10.DEL R398,R391,R367,R376 for For SSC_DPLL_REF_CLK and DPLL_REF_CLK debug 11. Reserve R72 to GND follow CRB Resrve 12. EC51 from 220uF change to 470uF for Lenovo Spec 13. ADD +USBVCC_SW3 of USB Discharge Circuit for Lenovo Spec 14. +V_3P3_MINI,USB Charger power,+USBVCC6 Circuit change for Lenovo require 15. U23 from APL5317 change to APL5611 for Inrush Current debug

0.3	2013/03/25	1 .R23,R24 change to 33 ohm for Audio FSOV Debug 2. R454 change to 0 ohm Follow WW9 PDG2.0 update 3. RJ21(2-3),RJ22(1-2),RJ23(2-3),RJ24(2-3) change to 0 ohm For Power LED debug 4. C581 change to 33pF for SLP_S3 debug 5. USBLAN change to Solid-state semiconductor For Lenovo spec 6. BOSS1,BOSS2 change to M2.0 For Lenovo spec 7. ADD C648,C160(2700pf) For Thermal debug 8. DEL R293,R305 For SIO change to 8602E/DX 9. ADD VR_READY POWER ON SEQUENCE Circuit For PCH_SYSPWROK Debug
1.0	2013/05/23	1. R272 from 150K change to 160K for match magic and MAG LAYERS choke(P.38) 2. RJ19 change to (2-3) For PWR_FAN function(P.18) 3. ADD R293,R305 RJ23,RJ24 change to (1-2) for PWR_FAN Function(P.27) 4. ADD C485(22uF) and EC37 For After Power loss debug(P.29) 5. Resrve R295 for Intel MOW 15 not support 2014 CPU(P.5) 6. Resrve SC19,SC20,SR12,SR15,SR14 For Intel MOW 15 not support 2014 CPU (P.7and P.8) 7. C100 (10uF) For Lenovo spec For VDD33 power noise debug(P.30) 8. RJ12 from (2-3) change to (1-2) for SIO form 8602DX change to 8602EX BOM selection(P.15) 9. R471 from 39 change to 47 ohm for SIO48M Monotonic debug(P.16) 10.R500 from 33 chnge to 51 ohm for HDA_BITCLK Monotonic debug(P.17) 11.ADD R314 (1K) For V_3P3_MINI Discharge debug(P.22) 12.Resrve R544 and R231,add R550(10K) Reserve For Lenovo spec require(P.22) 13.ADD R665 and R334, Resrve R467 for USBVCC_SW Drop debug(P.23) 14.RJ21 from (1-2) change to (2-3) ,RJ22 from (2-3) change to (1-2) for SIO from 8602DX change to 8602EX(P.27) 15.RJ23,RJ24 from (2-3) change to (1-2) PWR_FAN for Lenovo change to COM2(P.27) 16.ADD C518(10u) ,R609 from 300K change to 0 ohm, DEL C546,R610 from 0 change to 100K,R628 from 0 change to 300K,ADD C564(0.01uF)(P.37) 17. ADD C286(0.1uF)20130525 0.3 to 1.0 for VR_EN timing Debug (P.38)

			
Title REVISION HISTORY			
Size	Document Number	Rev	
Custom	H81H3-LM	1.0	
Date:	Friday, May 31, 2013	Sheet	43 of 43